ZYNQ UltraScale+ FPGA Development Board Z19-P

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2022-09-30	Wuhai Luo	First Release

Table of Contents

This MPSoCs FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX Zynq UltraScale+ EG chip ZU19EG solution, uses Processing System(PS)+Programmable Logic(PL) technology to integrate dual-core ARM ARM Cortex-A53 and FPGA programmable logic on a single chip. In addition, the core board has 5 pieces of 2GB DDR4 SDRAM, 1pcs of 32GB eMMC memory chip and 2pcs of 512Mb QSPI FLASH on PS side; and has 4pcs of 2GB DDR4 SDRAM on PL side.

On carrier board, there are a lot of interfaces, such as 2 FMC HPC interface, M.2 SSD interface, mini DP port, USB 3.0 typeC port, Gigabit Ethernet port, 2 Uart ports, TF card slot, JTAG port etc. It is a "professional" ZYNQ development platform for high-speed data transmission，exchange, pre-verification，post-application of data processing. it is very suitable for students, engineers and other groups engaged in MPSoCs development.

Part 1: FPGA Development Board Introduction

The following figure shows the block diagram of the entire development system:

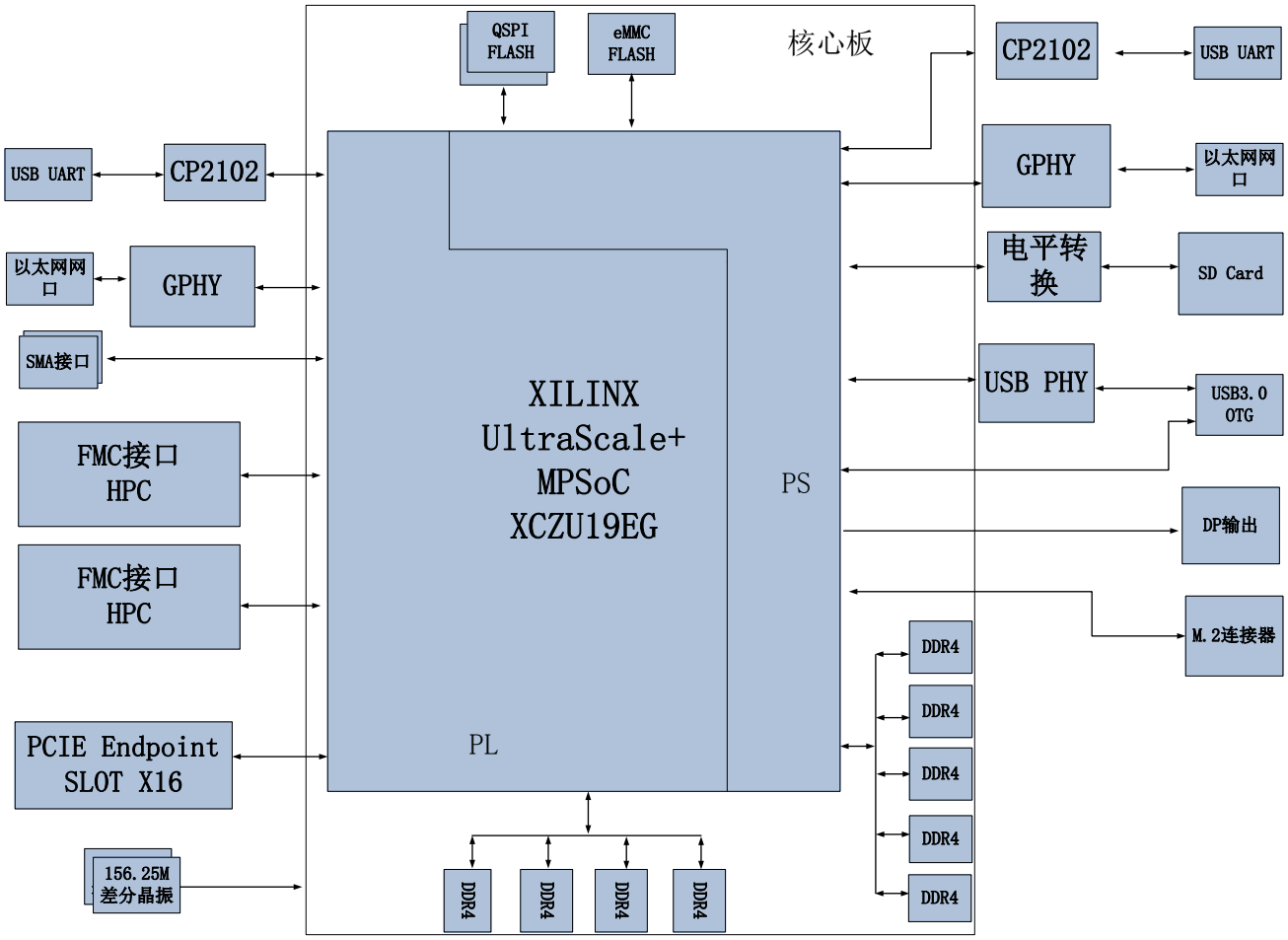


Figure 1-1-1: The Block Diagram of the Z19-P

Through the block diagram, we can see the main functions that the Z19-P FPGA Development Board contains:

- Z19 core board

  It consists of ZU19EG +10GB DDR4（PS）+8GB DDR4（PL）+32GB eMMC FLASH + 1Gb QSPI FLASH, and there are 2 crystal oscillators to provide the clock, a single-ended 33.3333MHz crystal oscillator for the PS system, and a differential 200MHz crystal oscillator for the PL

logic DDR reference clock.

- PCIE3.0 X16 Interface

  PCIE3.0 X16 endpoint interface, Z19-P board can be inserted in the PCIE SLOT of PC computer for data communication, with a communication speed of up to 8Gbps for each lane.

- M.2 Interface

  1 PCIEx1 standard M.2 interface, used to connect M.2 SSD solid state drives, with a communication speed of up to 6Gbps.

- DP Output Interface

  1 standard Display Port output display interface, used for video image display. Supports up to 4K@30Hz or 1080P@60Hz output

- USB 3.0 Interface

  One USB3.0 OTG interface, USB interface type is TYPE C. It can work in host mode, slave mode or OTG mode base on software driver.

- Gigabit Ethernet Interface

  One 10/100M/1000M Ethernet RJ45 ports on PS side for Ethernet data communication with computers or other network devices.

- USB Uart Interface

  Two Uart to USB ports, one for PS and another for PL. It is used to communicate with the computer, which is convenient for users to debug. The serial port chip adopts Silicon Labs CP2102GM's USB-UAR chip, and the USB interface adopts MINI USB interface.

- TF Card Slot Interface

  1 TF card socket, used to store LINUX image and system files.

- FMC Expansion Interface

  2 standard FMC HPC expansion port, which can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.).

- JTAG debug port

  A standard 10-pin 2.54mm JTAG debug ports. Users can debug and download firmware into the ZU19EG board through the JTAG cable.

- Temperature and humidity sensor chipset LM75

  On-board temperature and humidity sensor chipset of LM75, it is used to measure the temperature and humidity of the environment

- EEPROM

  One EEPROM 24LC04 with I2C interface

- Real Time Clock (RTC)

  1 built-in RTC real-time clock

- Different Clocks

  2 differential 156MHz crystal oscillator for GHT clock reference.

- LED Lights

  5 LEDs, include 1 LED on the core board, 4 LEDs on the carrier board. There is a power LED on the core board. There are 1 power LED,1 DONE LED and 2 user LED on the carrier board.

- KEYs

  One reset KEY.

Part 2: ACU19EG Core Board

Part 2.1: ACU19EG Core Board Introduction

ACU19EG (core board model name) FPGA core board, ZYNQ chipset is based on XCZU19EG-2FFVC1760I of XILINX company Zynq UltraScale+ MPSoCs EG Family.

This core board uses 9 Micron DDR4 chips MT40A512M16GE, 5 pcs DDR4 is on the PS side to form a 72-bit data bus bandwidth and 8GB capacity. 4 DDR4 chip is on the PL side, which is a 64-bit data bus width and a capacity of 8GB. The high-test speed of DDR4 SDRAM on the PS side and PL side is 1200MHz (data rate 2400Mbps). In addition, two 512MBit QSPI FLASH and an 32GB eMMC FLASH chip are also integrated on the core board.

Eight board-to-board connectors expand the IOs of USB2.0,Gigabit Ethernet, SD card and other MIOs in PS side; also expand 4 pairs of PS MGT, 48 GTH/GTY transceivers and almost all IO ports on the PL side (HP I/O:240，HD I/O：96). The core board size is 80*80 (mm), which is very suitable for secondary development.

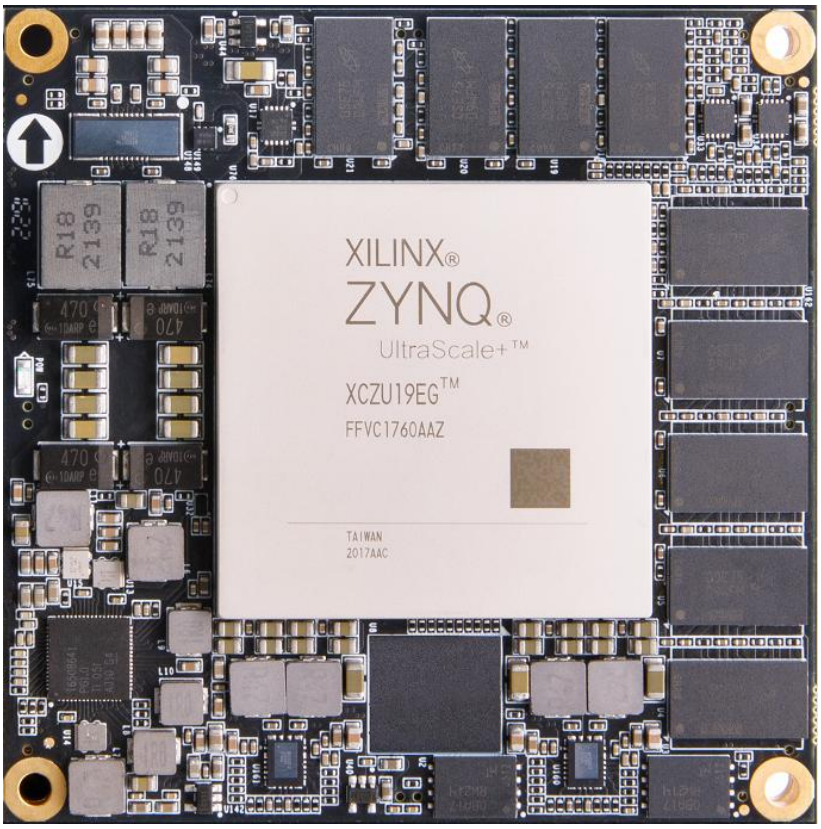


Figure 2-1-1: ACU19EG Core Board (Front View)

Part 2.2: MPSOC Chip

The core board ACU19EG uses Xilinx's Zynq UltraScale+ MPSoCs EG family chip:XCZU19EG-2FFVC1760I. The PS system of the ZU19EG chip integrates 4 ARM Cortex™-A53 processors with a speed of up to 1.3Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 533Mhz

The ZU19EG chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, with rich high-speed interfaces on the PS side such as PCIE Gen2, USB3.0, SATA 3.1, Display Port; it also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL side contains a wealth of programmable logic units, DSP and internal RAM. .

Figure 2-2-1 detailed the Overall Block Diagram of the ZU19EG Chipset.

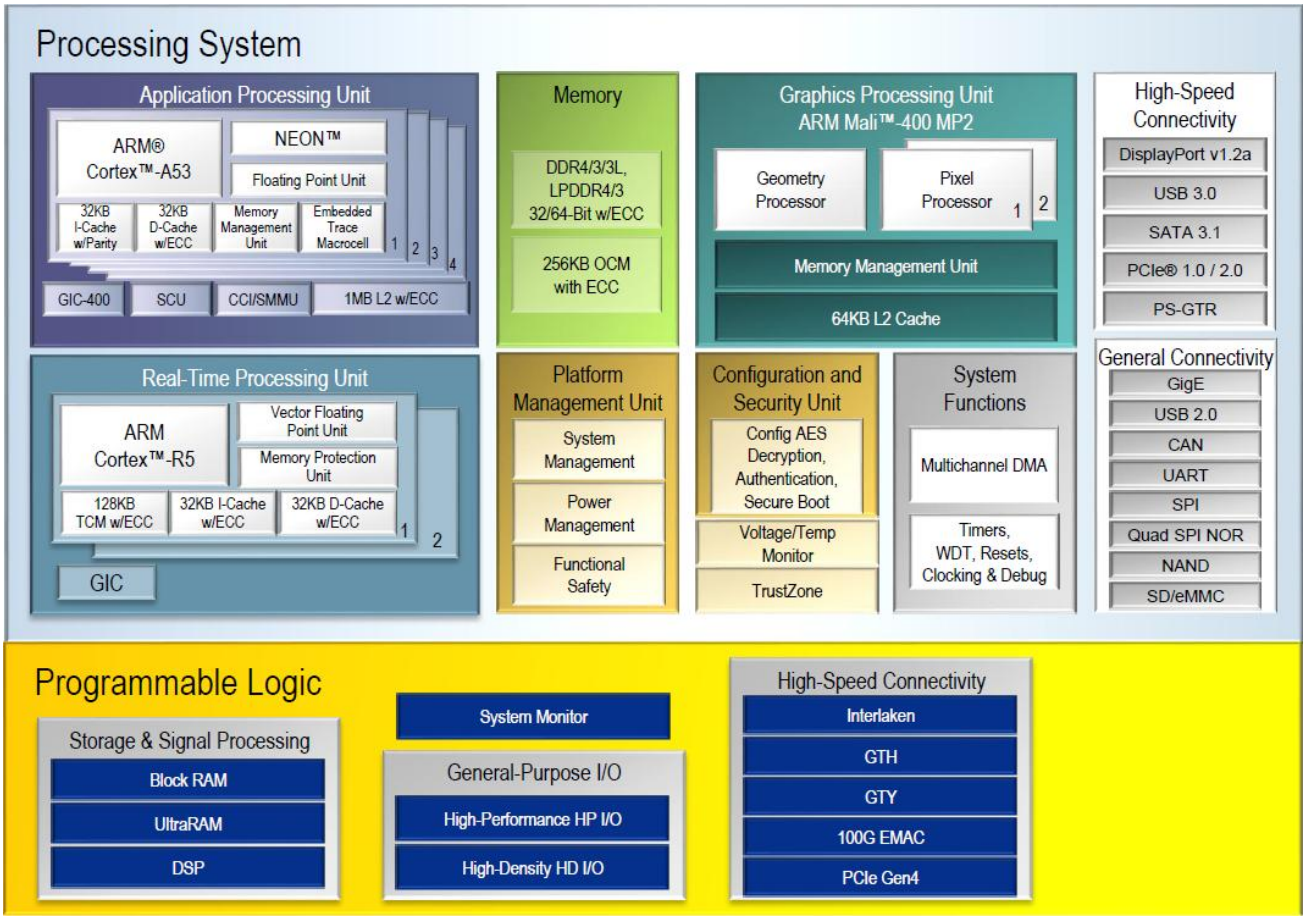


Figure 2-2-1: Overall Block Diagram of the ZYNQ ZU19EG Chipset

The main parameters of the PS system part are as follows:

- ARM quad-core Cortex™-A53 processor, speed up to 1.3GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs
- ARM dual-core Cortex-R5 processor, speed up to 533MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.
- External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface
- Static storage interface, support NAND, 2xQuad-SPI FLASH.
- High-speed connection interface, support PCIe Gen2 x 4, 2 x USB3.0,

Sata 3.1, Display Port, 4 x Tri-mode, Gigabit Ethernet

- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO
- Power management: Support the four-part division of power supply Full/Low/PL/Battery
- Encryption algorithm: support RSA, AES and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic part are as follows:

- Logic Cells: 1143K
- CLB Flip-flops: 1045K
- Look-up-tables (LUTs): 523K
- Block RAM: 34.6Mb
- Clock Management Units (CMTs): 11
- DSP Slices: 1968
- GTH 16.3Gb/s Transceiver: 44

XCZU19EG-2FFVC1760I chipset speed grade is -2, industrial grade, package is FFVC1760.

Part 2.3: DDR4 DRAM

There are 9pcs DDR4 SDRAM(MT40A512M16GE) on ACU19EG,5pcs DDR4 chipsets are on the PS side to form a 72-bit data bus bandwidth for supporting ECC function. 4pcs DDR4 chipsets is on the PL side to form 64-bit data bus bandwidth. The maximum speed of the DDR4 SDRAM on the PS side and PL side are both support 1200MHz (data rate 2400Mbps). The specific configuration of DDR4 SDRAM is shown in Table 2-3-1 below:

Position	Reference	Part number	Form	Factory
PS	U4,U5,U6,U7,U162	MT40A1G16KD-062E	1G x 6bit	Micron
PL	U18,U19,U20,U21	MT40A1G16KD-062E	1G x 6bit	Micron

Table 2-3-1: DDR4 SDRAM Configuration

The block diagram of DDR4 SDRAM on the PS Side is shown in Figure 2-3-1:

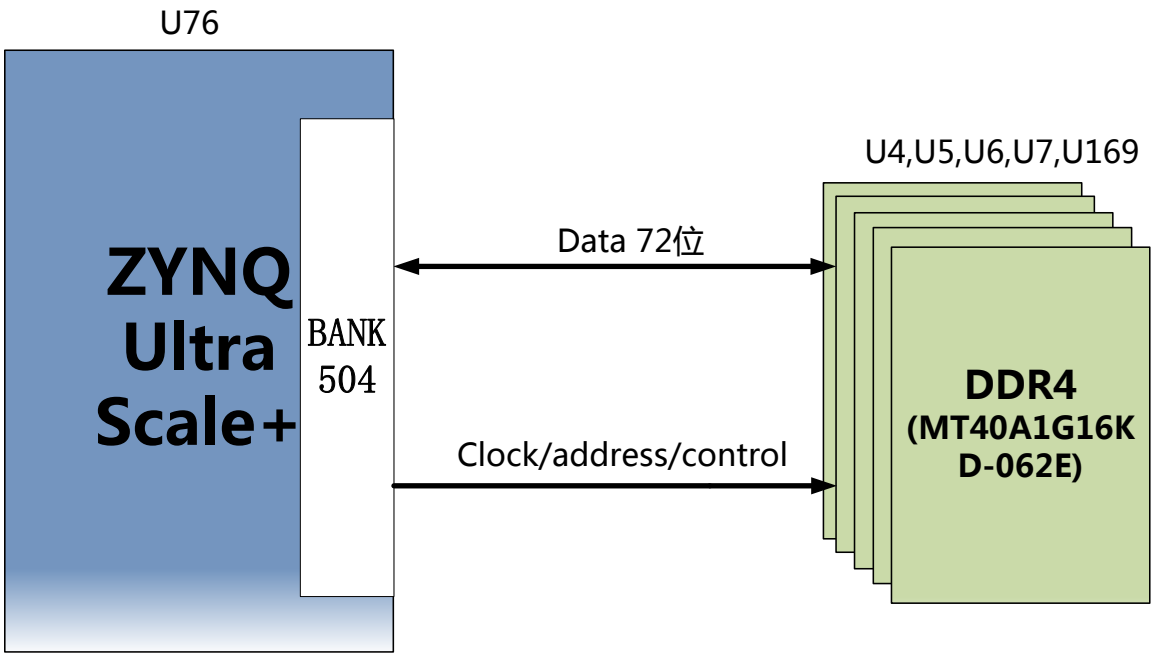


Figure 2-3-1: PS DDR4 DRAM block diagram

The block diagram of DDR4 SDRAM on the PL Side is shown in Figure 2-3-2:

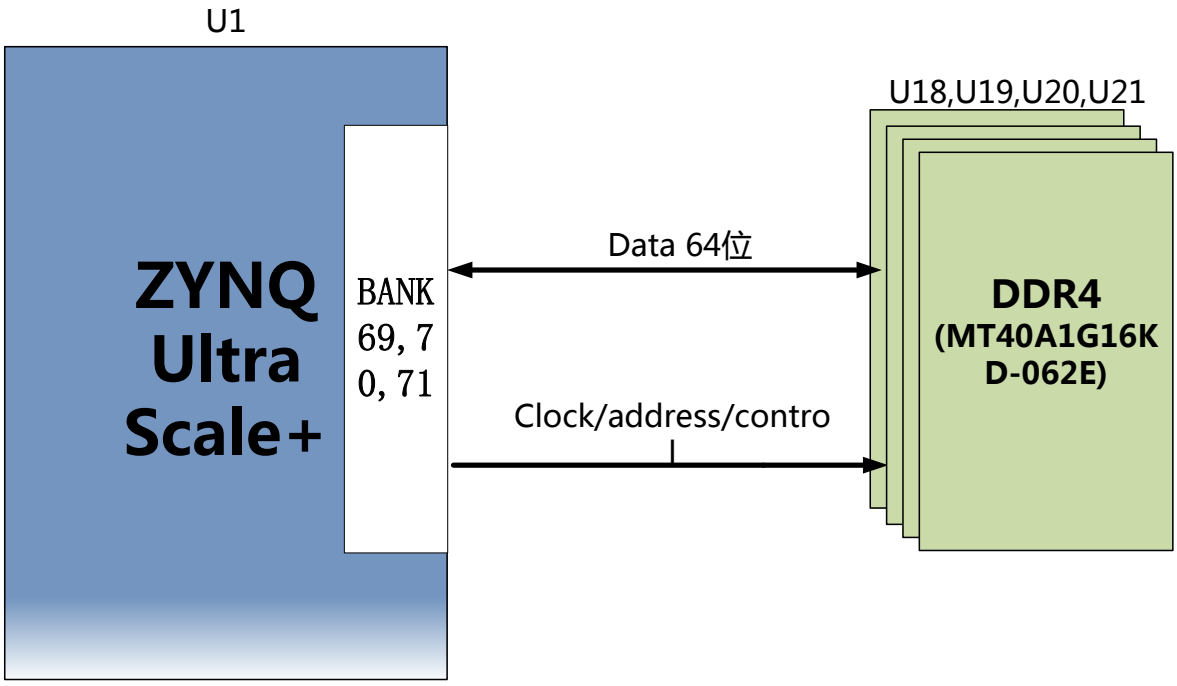


Figure 2-3-2: PL DDR4 DRAM block diagram

PS Side DDR4 DRAM pin assignment:

Signal name	Pin name	Pin number
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	BA30
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AY30
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AY33
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AY32
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AT30
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AR30
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AT32
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AR32
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	AR40
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	AP40
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	AK37
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	AJ37
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	AU41
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	AU40
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	AL41
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	AL40

PS_DDR4_DQS8_N	PS_DDR_DQS_N8_504	AY40
PS_DDR4_DQS8_P	PS_DDR_DQS_P8_504	AY39
PS_DDR4_DQ0	PS_DDR_DQ0_504	AV29
PS_DDR4_DQ1	PS_DDR_DQ1_504	AW30
PS_DDR4_DQ2	PS_DDR_DQ2_504	AW29
PS_DDR4_DQ3	PS_DDR_DQ3_504	AW31
PS_DDR4_DQ4	PS_DDR_DQ4_504	BB31
PS_DDR4_DQ5	PS_DDR_DQ5_504	BB30
PS_DDR4_DQ6	PS_DDR_DQ6_504	BB29
PS_DDR4_DQ7	PS_DDR_DQ7_504	BA31
PS_DDR4_DQ8	PS_DDR_DQ8_504	BB33
PS_DDR4_DQ9	PS_DDR_DQ9_504	BA32
PS_DDR4_DQ10	PS_DDR_DQ10_504	BA33
PS_DDR4_DQ11	PS_DDR_DQ11_504	BB34
PS_DDR4_DQ12	PS_DDR_DQ12_504	AV31
PS_DDR4_DQ13	PS_DDR_DQ13_504	AW32
PS_DDR4_DQ14	PS_DDR_DQ14_504	AV32
PS_DDR4_DQ15	PS_DDR_DQ15_504	AV33
PS_DDR4_DQ16	PS_DDR_DQ16_504	AN29
PS_DDR4_DQ17	PS_DDR_DQ17_504	AP29
PS_DDR4_DQ18	PS_DDR_DQ18_504	AP30
PS_DDR4_DQ19	PS_DDR_DQ19_504	AP31
PS_DDR4_DQ20	PS_DDR_DQ20_504	AT31
PS_DDR4_DQ21	PS_DDR_DQ21_504	AU30
PS_DDR4_DQ22	PS_DDR_DQ22_504	AU31
PS_DDR4_DQ23	PS_DDR_DQ23_504	AU29
PS_DDR4_DQ24	PS_DDR_DQ24_504	AV34
PS_DDR4_DQ25	PS_DDR_DQ25_504	AU33
PS_DDR4_DQ26	PS_DDR_DQ26_504	AT33
PS_DDR4_DQ27	PS_DDR_DQ27_504	AU34
PS_DDR4_DQ28	PS_DDR_DQ28_504	AN33
PS_DDR4_DQ29	PS_DDR_DQ29_504	AP32
PS_DDR4_DQ30	PS_DDR_DQ30_504	AN32
PS_DDR4_DQ31	PS_DDR_DQ31_504	AN31

PS_DDR4_DQ32	PS_DDR_DQ32_504	AN41
PS_DDR4_DQ33	PS_DDR_DQ33_504	AN42
PS_DDR4_DQ34	PS_DDR_DQ34_504	AP42
PS_DDR4_DQ35	PS_DDR_DQ35_504	AP41
PS_DDR4_DQ36	PS_DDR_DQ36_504	AN39
PS_DDR4_DQ37	PS_DDR_DQ37_504	AR38
PS_DDR4_DQ38	PS_DDR_DQ38_504	AP39
PS_DDR4_DQ39	PS_DDR_DQ39_504	AN38
PS_DDR4_DQ40	PS_DDR_DQ40_504	AL37
PS_DDR4_DQ41	PS_DDR_DQ41_504	AL38
PS_DDR4_DQ42	PS_DDR_DQ42_504	AK38
PS_DDR4_DQ43	PS_DDR_DQ43_504	AK39
PS_DDR4_DQ44	PS_DDR_DQ44_504	AJ36
PS_DDR4_DQ45	PS_DDR_DQ45_504	AL35
PS_DDR4_DQ46	PS_DDR_DQ46_504	AJ35
PS_DDR4_DQ47	PS_DDR_DQ47_504	AK35
PS_DDR4_DQ48	PS_DDR_DQ48_504	AR42
PS_DDR4_DQ49	PS_DDR_DQ49_504	AT41
PS_DDR4_DQ50	PS_DDR_DQ50_504	AT42
PS_DDR4_DQ51	PS_DDR_DQ51_504	AT40
PS_DDR4_DQ52	PS_DDR_DQ52_504	AV42
PS_DDR4_DQ53	PS_DDR_DQ53_504	AV41
PS_DDR4_DQ54	PS_DDR_DQ54_504	AV39
PS_DDR4_DQ55	PS_DDR_DQ55_504	AV38
PS_DDR4_DQ56	PS_DDR_DQ56_504	AM39
PS_DDR4_DQ57	PS_DDR_DQ57_504	AM38
PS_DDR4_DQ58	PS_DDR_DQ58_504	AM40
PS_DDR4_DQ59	PS_DDR_DQ59_504	AM41
PS_DDR4_DQ60	PS_DDR_DQ60_504	AJ42
PS_DDR4_DQ61	PS_DDR_DQ61_504	AK42
PS_DDR4_DQ62	PS_DDR_DQ62_504	AK40
PS_DDR4_DQ63	PS_DDR_DQ63_504	AK41
PS_DDR4_DQ64	PS_DDR4_DQ64_504	BB40
PS_DDR4_DQ65	PS_DDR4_DQ65_504	BA41

PS_DDR4_DQ66	PS_DDR4_DQ66_504	BA42
PS_DDR4_DQ67	PS_DDR4_DQ67_504	BA40
PS_DDR4_DQ68	PS_DDR4_DQ68_504	AW42
PS_DDR4_DQ69	PS_DDR4_DQ69_504	AW40
PS_DDR4_DQ70	PS_DDR4_DQ70_504	AW41
PS_DDR4_DQ71	PS_DDR4_DQ71_504	AW39
PS_DDR4_DM0	PS_DDR_DM0_504	AY29
PS_DDR4_DM1	PS_DDR_DM1_504	AY34
PS_DDR4_DM2	PS_DDR_DM2_504	AR29
PS_DDR4_DM3	PS_DDR_DM3_504	AR33
PS_DDR4_DM4	PS_DDR_DM4_504	AR39
PS_DDR4_DM5	PS_DDR_DM5_504	AL36
PS_DDR4_DM6	PS_DDR_DM6_504	AU39
PS_DDR4_DM7	PS_DDR_DM7_504	AL42
PS_DDR4_DM8	PS_DDR_DM8_504	AY42
PS_DDR4_A0	PS_DDR_A0_504	BA38
PS_DDR4_A1	PS_DDR_A1_504	BB36
PS_DDR4_A2	PS_DDR_A2_504	BA35
PS_DDR4_A3	PS_DDR_A3_504	BB35
PS_DDR4_A4	PS_DDR_A4_504	BB38
PS_DDR4_A5	PS_DDR_A5_504	AY35
PS_DDR4_A6	PS_DDR_A6_504	AP37
PS_DDR4_A7	PS_DDR_A7_504	AT36
PS_DDR4_A8	PS_DDR_A8_504	AR35
PS_DDR4_A9	PS_DDR_A9_504	AT35
PS_DDR4_A10	PS_DDR_A10_504	AU35
PS_DDR4_A11	PS_DDR_A11_504	AU36
PS_DDR4_A12	PS_DDR_A12_504	AW36
PS_DDR4_A13	PS_DDR_A13_504	AW37
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	AR37
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	AM36
PS_DDR4_BA0	PS_DDR_BA0_504	AN37
PS_DDR4_BA1	PS_DDR_BA1_504	AN36
PS_DDR4_BG0	PS_DDR_BG0_504	AP36

PS_DDR4_CAS_B	PS_DDR_A15_504	AW34
PS_DDR4_CKE0	PS_DDR_CKE0_504	AY38
PS_DDR4_CLK0_N	PS_DDR_CK_N0_504	BA37
PS_DDR4_CLK0_P	PS_DDR_CK0_504	BA36
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	AY37
PS_DDR4_ODT0	PS_DDR_ODT0_504	BB39
PS_DDR4_PARITY	PS_DDR_PARITY_504	AM35
PS_DDR4_RAS_B	PS_DDR_A16_504	AR34
PS_DDR4_RESET_B	PS_DDR_RAM_RST_N_504	AM34
PS_DDR4_WE_B	PS_DDR_A14_504	AW35

PL Side DDR4 SDRAM pin assignment:

Signal name	Pin name	Pin number
PL_DDR4_DQS0_N	IO_L10N_T1U_N7_QBC_AD4N_70	G23
PL_DDR4_DQS0_P	IO_L10P_T1U_N6_QBC_AD4P_70	H23
PL_DDR4_DQS1_N	IO_L4N_T0U_N7_DBC_AD7N_70	K24
PL_DDR4_DQS1_P	IO_L4P_T0U_N6_DBC_AD7P_70	L24
PL_DDR4_DQS2_N	IO_L22N_T3U_N7_DBC_AD0N_70	B26
PL_DDR4_DQS2_P	IO_L22P_T3U_N6_DBC_AD0P_70	B25
PL_DDR4_DQS3_N	IO_L16N_T2U_N7_QBC_AD3N_70	E27
PL_DDR4_DQS3_P	IO_L16P_T2U_N6_QBC_AD3P_70	E26
PL_DDR4_DQS4_N	IO_L10N_T1U_N7_QBC_AD4N_69	A32
PL_DDR4_DQS4_P	IO_L10P_T1U_N6_QBC_AD4P_69	B31
PL_DDR4_DQS5_N	IO_L4N_T0U_N7_DBC_AD7N_69	F30
PL_DDR4_DQS5_P	IO_L4P_T0U_N6_DBC_AD7P_69	G30
PL_DDR4_DQS6_N	IO_L22N_T3U_N7_DBC_AD0N_69	A40
PL_DDR4_DQS6_P	IO_L22P_T3U_N6_DBC_AD0P_69	A39
PL_DDR4_DQS7_N	IO_L16N_T2U_N7_QBC_AD3N_69	C34
PL_DDR4_DQS7_P	IO_L16P_T2U_N6_QBC_AD3P_69	D34
PL_DDR4_DQ0	IO_L12N_T1U_N11_GC_70	G25
PL_DDR4_DQ1	IO_L9N_T1L_N5_AD12N_70	J24
PL_DDR4_DQ2	IO_L11P_T1U_N8_GC_70	H25
PL_DDR4_DQ3	IO_L8N_T1L_N3_AD5N_70	J26
PL_DDR4_DQ4	IO_L12P_T1U_N10_GC_70	H24

PL_DDR4_DQ5	IO_L8P_T1L_N2_AD5P_70	K26
PL_DDR4_DQ6	IO_L11N_T1U_N9_GC_70	H26
PL_DDR4_DQ7	IO_L9P_T1L_N4_AD12P_70	J23
PL_DDR4_DQ8	IO_L2P_T0L_N2_70	M25
PL_DDR4_DQ9	IO_L6P_T0U_N10_AD6P_70	M23
PL_DDR4_DQ10	IO_L2N_T0L_N3_70	L25
PL_DDR4_DQ11	IO_L6N_T0U_N11_AD6N_70	L23
PL_DDR4_DQ12	IO_L3P_T0L_N4_AD15P_70	N24
PL_DDR4_DQ13	IO_L5N_T0U_N9_AD14N_70	N23
PL_DDR4_DQ14	IO_L3N_T0L_N5_AD15N_70	N25
PL_DDR4_DQ15	IO_L5P_T0U_N8_AD14P_70	P23
PL_DDR4_DQ16	IO_L20N_T3L_N3_AD1N_70	A28
PL_DDR4_DQ17	IO_L24P_T3U_N10_70	A24
PL_DDR4_DQ18	IO_L21N_T3L_N5_AD8N_70	B27
PL_DDR4_DQ19	IO_L23N_T3U_N9_70	C25
PL_DDR4_DQ20	IO_L20P_T3L_N2_AD1P_70	A27
PL_DDR4_DQ21	IO_L21P_T3L_N4_AD8P_70	C26
PL_DDR4_DQ22	IO_L24N_T3U_N11_70	A25
PL_DDR4_DQ23	IO_L23P_T3U_N8_70	C24
PL_DDR4_DQ24	IO_L15P_T2L_N4_AD11P_70	F27
PL_DDR4_DQ25	IO_L14P_T2L_N2_GC_70	F25
PL_DDR4_DQ26	IO_L17P_T2U_N8_AD10P_70	D27
PL_DDR4_DQ27	IO_L14N_T2L_N3_GC_70	E25
PL_DDR4_DQ28	IO_L15N_T2L_N5_AD11N_70	F28
PL_DDR4_DQ29	IO_L18P_T2U_N10_AD2P_70	F24
PL_DDR4_DQ30	IO_L17N_T2U_N9_AD10N_70	D28
PL_DDR4_DQ31	IO_L18N_T2U_N11_AD2N_70	E24
PL_DDR4_DQ32	IO_L11N_T1U_N9_GC_69	D31
PL_DDR4_DQ33	IO_L9P_T1L_N4_AD12P_69	A29
PL_DDR4_DQ34	IO_L12P_T1U_N10_GC_69	C30
PL_DDR4_DQ35	IO_L9N_T1L_N5_AD12N_69	A30
PL_DDR4_DQ36	IO_L11P_T1U_N8_GC_69	E31
PL_DDR4_DQ37	IO_L8P_T1L_N2_AD5P_69	C29
PL_DDR4_DQ38	IO_L12N_T1U_N11_GC_69	C31

PL_DDR4_DQ39	IO_L8N_T1L_N3_AD5N_69	B30
PL_DDR4_DQ40	IO_L3N_T0L_N5_AD15N_69	F32
PL_DDR4_DQ41	IO_L5P_T0U_N8_AD14P_69	G28
PL_DDR4_DQ42	IO_L2N_T0L_N3_69	H30
PL_DDR4_DQ43	IO_L6P_T0U_N10_AD6P_69	J28
PL_DDR4_DQ44	IO_L2P_T0L_N2_69	J30
PL_DDR4_DQ45	IO_L6N_T0U_N11_AD6N_69	H28
PL_DDR4_DQ46	IO_L3P_T0L_N4_AD15P_69	F31
PL_DDR4_DQ47	IO_L5N_T0U_N9_AD14N_69	F29
PL_DDR4_DQ48	IO_L24P_T3U_N10_69	C42
PL_DDR4_DQ49	IO_L21N_T3L_N5_AD8N_69	A38
PL_DDR4_DQ50	IO_L23P_T3U_N8_69	B40
PL_DDR4_DQ51	IO_L20N_T3L_N3_AD1N_69	B37
PL_DDR4_DQ52	IO_L24N_T3U_N11_69	B42
PL_DDR4_DQ53	IO_L20P_T3L_N2_AD1P_69	B36
PL_DDR4_DQ54	IO_L23N_T3U_N9_69	B41
PL_DDR4_DQ55	IO_L21P_T3L_N4_AD8P_69	A37
PL_DDR4_DQ56	IO_L15N_T2L_N5_AD11N_69	C33
PL_DDR4_DQ57	IO_L17N_T2U_N9_AD10N_69	A35
PL_DDR4_DQ58	IO_L15P_T2L_N4_AD11P_69	D33
PL_DDR4_DQ59	IO_L14N_T2L_N3_GC_69	B33
PL_DDR4_DQ60	IO_L14P_T2L_N2_GC_69	B32
PL_DDR4_DQ61	IO_L18N_T2U_N11_AD2N_69	A34
PL_DDR4_DQ62	IO_L17P_T2U_N8_AD10P_69	B35
PL_DDR4_DQ63	IO_L18P_T2U_N10_AD2P_69	A33
PL_DDR4_DM0	IO_L7P_T1L_N0_QBC_AD13P_70	K27
PL_DDR4_DM1	IO_L1P_T0L_N0_DBC_70	P26
PL_DDR4_DM2	IO_L19P_T3L_N0_DBC_AD9P_70	C28
PL_DDR4_DM3	IO_L13P_T2L_N0_GC_QBC_70	G26
PL_DDR4_DM4	IO_L7P_T1L_N0_QBC_AD13P_69	E29
PL_DDR4_DM5	IO_L1P_T0L_N0_DBC_69	K29
PL_DDR4_DM6	IO_L19P_T3L_N0_DBC_AD9P_69	C36
PL_DDR4_DM7	IO_L13P_T2L_N0_GC_QBC_69	E32
PL_DDR4_A0	IO_L6N_T0U_N11_AD6N_71	M21

PL_DDR4_A1	IO_L5N_T0U_N9_AD14N_71	N21
PL_DDR4_A2	IO_L16N_T2U_N7_QBC_AD3N_71	E20
PL_DDR4_A3	IO_L5P_T0U_N8_AD14P_71	P21
PL_DDR4_A4	IO_L17P_T2U_N8_AD10P_71	E21
PL_DDR4_A5	IO_L15N_T2L_N5_AD11N_71	E19
PL_DDR4_A6	IO_L6P_T0U_N10_AD6P_71	M22
PL_DDR4_A7	IO_L7N_T1L_N1_QBC_AD13N_71	J19
PL_DDR4_A8	IO_L9N_T1L_N5_AD12N_71	J21
PL_DDR4_A9	IO_L16P_T2U_N6_QBC_AD3P_71	F20
PL_DDR4_A10	IO_L8P_T1L_N2_AD5P_71	L20
PL_DDR4_A11	IO_L3P_T0L_N4_AD15P_71	M20
PL_DDR4_A12	IO_L4P_T0U_N6_DBC_AD7P_71	N20
PL_DDR4_A13	IO_L7P_T1L_N0_QBC_AD13P_71	K19
PL_DDR4_CS_B	IO_L4N_T0U_N7_DBC_AD7N_71	N19
PL_DDR4_ACT_B	IO_L8N_T1L_N3_AD5N_71	K20
PL_DDR4_ODT	IO_L9P_T1L_N4_AD12P_71	K21
PL_DDR4_WE_B	IO_L10N_T1U_N7_QBC_AD4N_71	J22
PL_DDR4_BA0	IO_L10P_T1U_N6_QBC_AD4P_71	K22
PL_DDR4_BA1	IO_L15P_T2L_N4_AD11P_71	F19
PL_DDR4_CAS_B	IO_L11N_T1U_N9_GC_71	H19
PL_DDR4_RAS_B	IO_L11P_T1U_N8_GC_71	H20
PL_DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_71	G21
PL_DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_71	G22
PL_DDR4_BG0	IO_L14N_T2L_N3_GC_71	F22
PL_DDR4_CKE	IO_L17N_T2U_N9_AD10N_71	D21
PL_DDR4_RST	IO_L14P_T2L_N2_GC_71	F23

Part 2.4: QSPI Flash

The ACU19EG has two 512MBit Quad-SPI FLASH chip to form an 8-bit data bus width, the flash model is MT25QU512ABB1EW9-0SIT.

The chipset name and related parameters of QSPI FLASH are shown in Table 2-4-1.

Reference	Part number	Capacity	Factory
U2,U3	MT25QU512ABB1EW9-0SIT	512M bit	Micron

Table 2-4-1: QSPI FLASH Specification

Figure 2-4-1 shows the QSPI Flash in the schematic.

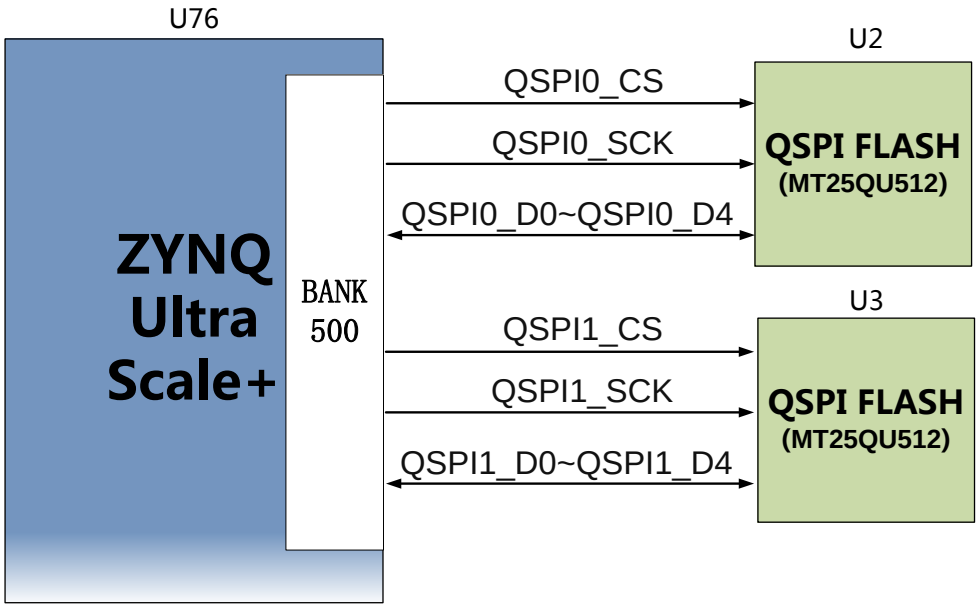


Figure 2-4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	Pin Name	Pin Number
MIO5_QSPI0_SS_B	PS_MIO5_500	AL32
MIO0_QSPI0_SCLK	PS_MIO0_500	AM33
MIO4_QSPI0_IO0	PS_MIO4_500	AL33
MIO1_QSPI0_IO1	PS_MIO1_500	AM29
MIO2_QSPI0_IO2	PS_MIO2_500	AM31
MIO3_QSPI0_IO3	PS_MIO3_500	AM30
MIO7_QSPI1_SS_B	PS_MIO7_500	AL30
MIO12_QSPI1_SCLK	PS_MIO12_500	AJ34
MIO8_QSPI1_IO0	PS_MIO8_500	AK33
MIO9_QSPI1_IO1	PS_MIO9_500	AK34
MIO10_QSPI1_IO2	PS_MIO10_500	AK30
MIO11_QSPI1_IO3	PS_MIO11_500	AK32

Part 2.5: eMMC Flash

The ACU19EG core board is mounted with a 32GB eMMC FLASH, the part number is MTFC32GAPALBH-IT. The data width of eMMC FLASH is 8bit. The chipset name and related parameters of eMMC FLASH are shown in Table 2-5-1.

Reference	Part Number	Capacity	Factory
U8	MTFC32GAPALBH-IT	32G Byte	Micron

Table 2-5-1: eMMC FLASH Specification

The eMMC FLASH is connected to MIOs PS side of the ZYNQ UltraScale+. Figure 2-5-1 shows the part of eMMC Flash in the schematic diagram.

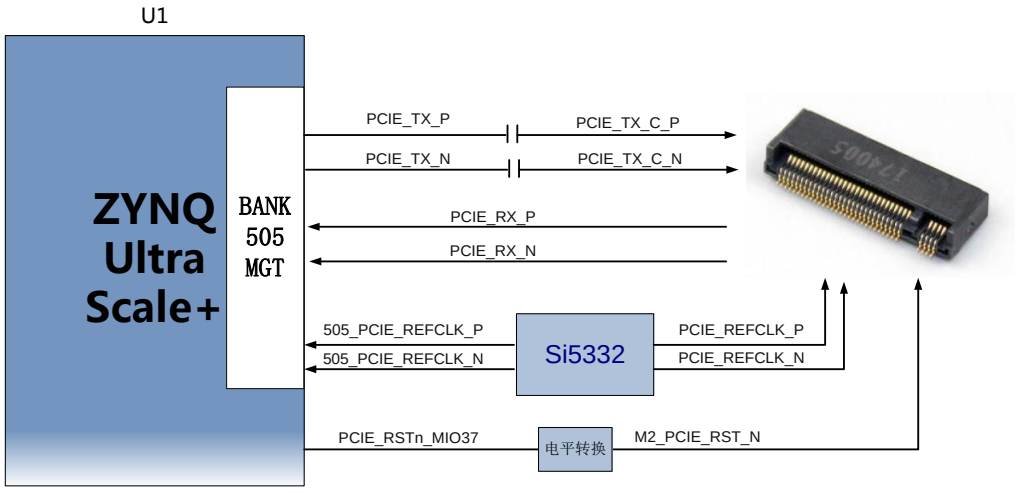


Figure 2-5-1: eMMC Flash in the schematic

Configuration Chip pin assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO22_500	AH32
MMC_CMD	PS_MIO21_500	AF35
MMC_DAT0	PS_MIO13_500	AD34
MMC_DAT1	PS_MIO14_500	AJ32

MMC_DAT2	PS_MIO15_500	AD35
MMC_DAT3	PS_MIO16_500	AJ31
MMC_DAT4	PS_MIO17_500	AJ30
MMC_DAT5	PS_MIO18_500	AE34
MMC_DAT6	PS_MIO19_500	AE35
MMC_DAT7	PS_MIO20_500	AH34
MMC_RSTN	PS_MIO23_500	AG35

Part 2.6: Clock configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 2-6-1:

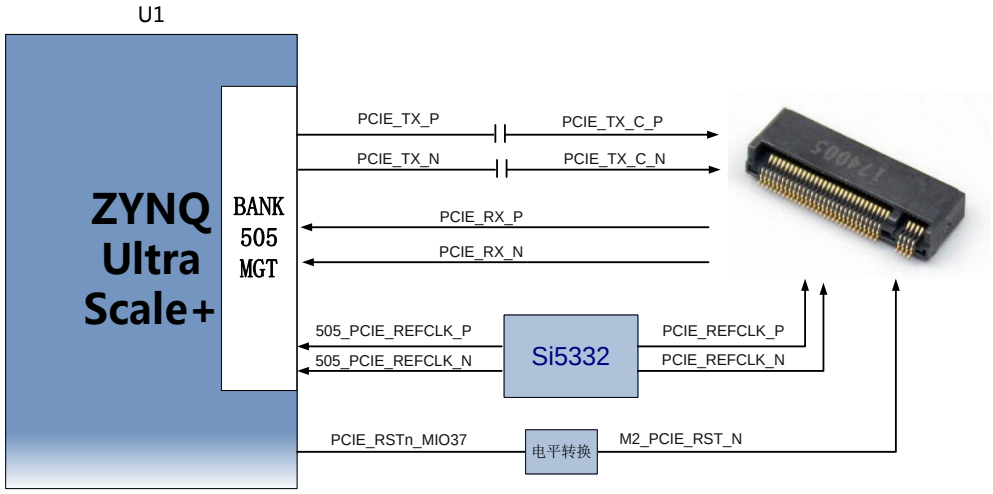


Figure 2-6-1: Core Board Clock Source

PS System RTC Real Time Clock

The crystal of Y1 on the core board provides a 32.768KHz clock source for the RTC real-time. The schematic diagram is shown in Figure 2-6-2:

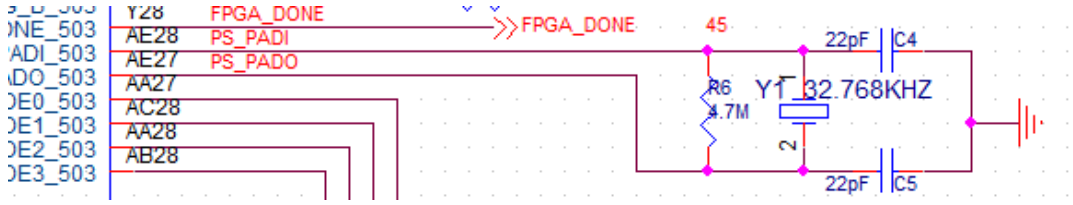


Figure 2-6-2: Crystal Oscillator for RTC

Clock pin assignment:

Signal Name	Pin
PS_PADI_503	**AE28**
PS_PADO_503	**AE27**

PS System Clock Source

The X1 crystal on the core board provides a 33.333MHz clock input for the PS part. The clock input is connected to the PS_REF_CLK_503 pin of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-3:

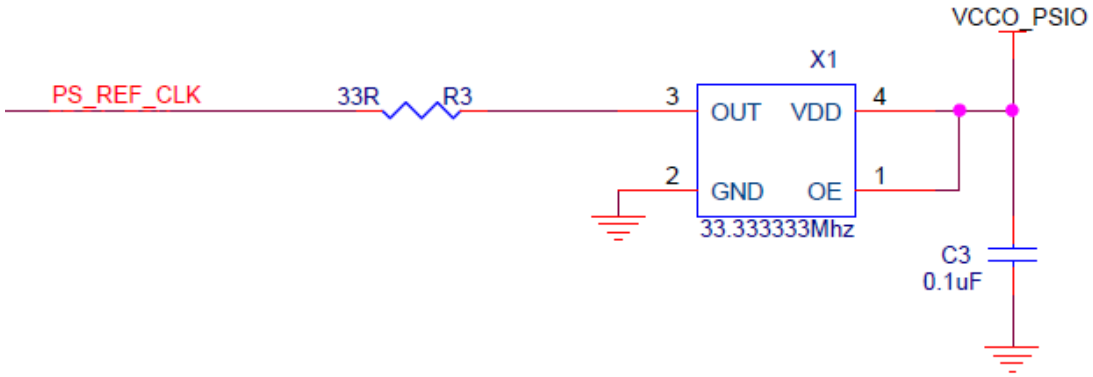


Figure 2-6-3: Active Crystal in PS part

Clock pin assignment:

Signal Name	Pin
PS_REF_CLK	**AC27**

PL System Clock Source

The core board provides a differential 200MHz clock source for the reference clock of the DDR4 controller. The clock is connected to the global clock (MRCC) of PL BANK71. The schematic diagram of this clock source is shown in Figure 2-6-4

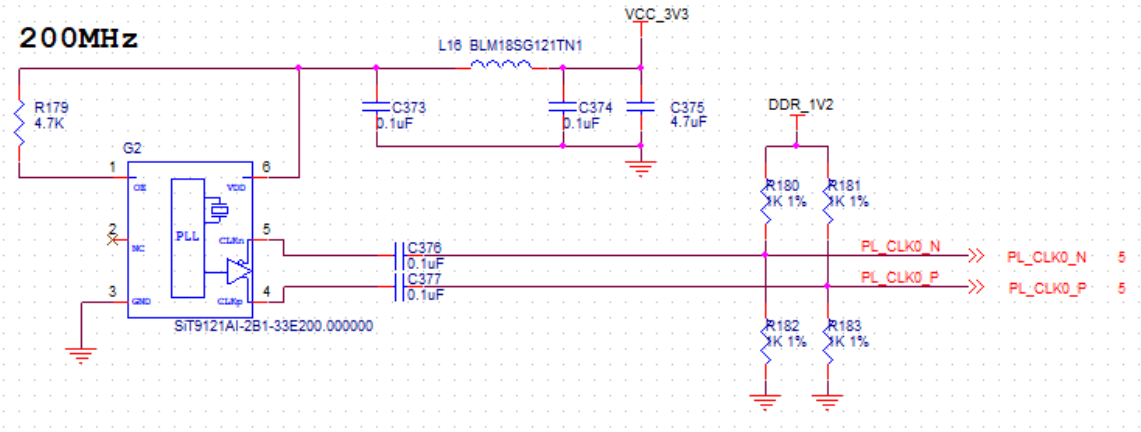


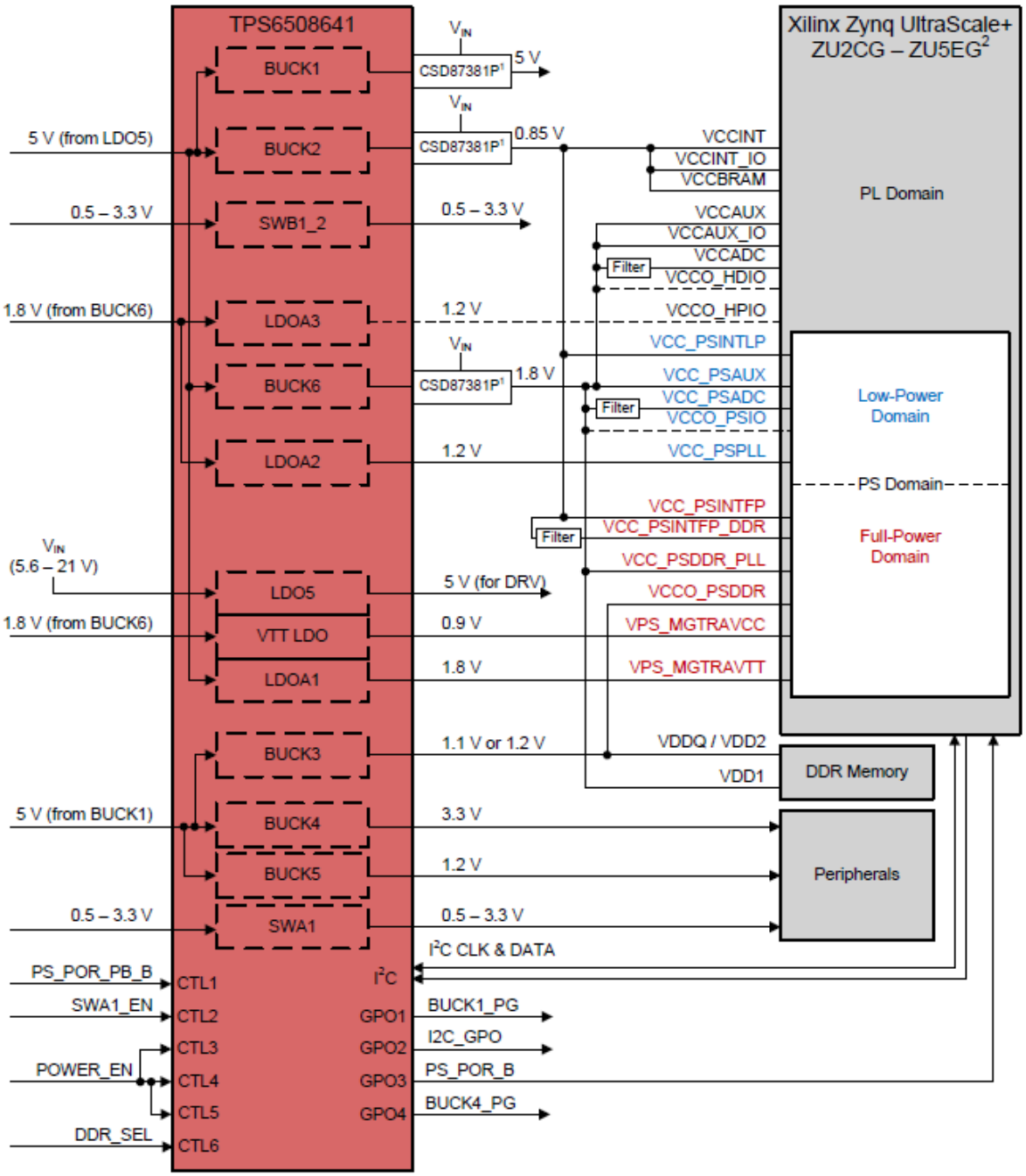
Figure 2-6-4: PL system clock source

Clock pin assignment:

Signal Name	Pin
PL_CLK0_P	H21
PL_CLK0_N	G20

Part 2.7: Power Supply

The power supply voltage of the ACU19EG core board is DC12V, which is supplied by the carrier board. The core board uses a DC/DC power of MAX20796GFB+ to provide the core power of 0.85V. a PMIC chip TPS6508640 is used to generate all other power supplies required by the XCZU9EG chip. For the TPS6508640 power supply design, please refer to the power supply chip manual. The design block diagram is as follows :


TPS6508641
BUCK1
BUCK2
SWB1_2
LDOA3
BUCK6
LDOA2
LDO5
VTT LDO
LDOA1
BUCK3
BUCK4
BUCK5
SWA1
CTL1
CTL2
CTL3
CTL4
CTL5
CTL6
I²C
GPO1
GPO2
GPO3
GPO4
VIN
CSD87381P
5 V
0.85 V
0.5 – 3.3 V
1.2 V
1.8 V
5 V (for DRV)
0.9 V
1.1 V or 1.2 V
3.3 V
5 V (from LDO5)
1.8 V (from BUCK6)
VIN (5.6 – 21 V)
5 V (from BUCK1)
PS_POR_PB_B
SWA1_EN
POWER_EN
DDR_SEL
I²C CLK & DATA
BUCK1_PG
I2C_GPO
PS_POR_B
BUCK4_PG
Xilinx Zynq UltraScale+ ZU2CG – ZU5EG²
PL Domain
Low-Power Domain
PS Domain
Full-Power Domain
Filter
VCCINT
VCCINT_IO
VCCBRAM
VCCAUX
VCCAUX_IO
VCCADC
VCCO_HDIO
VCCO_HPIO
VCC_PSINTLP
VCC_PSAUX
VCC_PSADC
VCCO_PSIO
VCC_PSPLL
VCC_PSINTFP
VCC_PSINTFP_DDR
VCC_PSDDR_PLL
VCCO_PSDDR
VPS_MGTRAVCC
VPS_MGTRAVTT
VDDQ / VDD2
VDD1
DDR Memory
Peripherals

Part 2.8: ACU19EG Core Board Form Factors

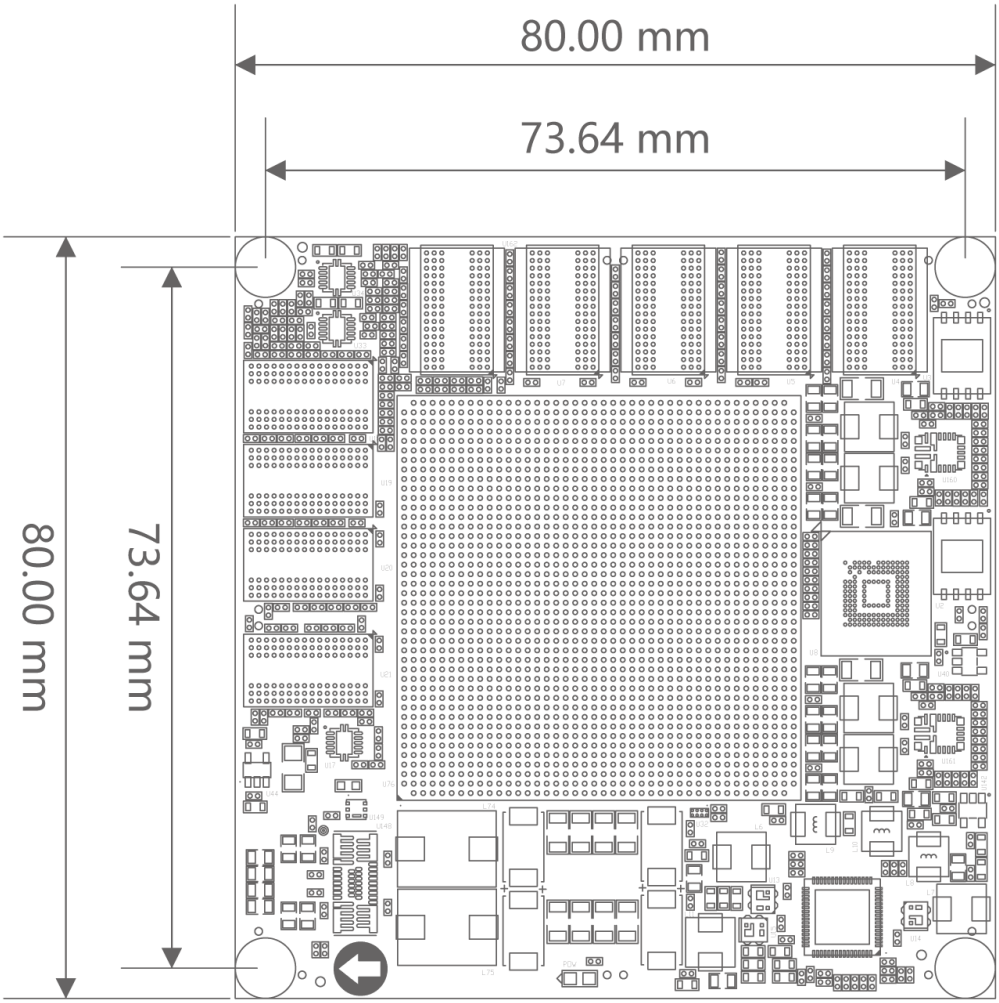


Figure 2-8-1: ACU19EG Core Board Form Factors

Part 2.10: Board to Board Connectors pin assignment

The core board has eight high-speed board-to-board connectors. It uses 120-pin connectors (J29~J36) to connect to the carrier board. The connectors used is Panasonic AXK5A2137YG, and the connector in the carrier board is Panasonic AXK6A2337YG.

J29 connector

J29 connects the GTX signal of BANK128，129，130，131;

Pin assignment of board to board connector J29

J29 Pin	Signal Name	Pin Number	J29 Pin	Signal Name	Pin Number
1	131_CLK0_P	L32	2	131_CLK1_P	J32
3	131_CLK0_N	L33	4	131_CLK1_N	J33
5	GND		6	GND	
7	131_RX3_P	D39	8	131_TX3_P	E36
9	131_RX3_N	D40	10	131_TX3_N	E37
11	GND		12	GND	
13	131_RX2_P	E41	14	131_TX2_P	F34
15	131_RX2_N	E42	16	131_TX2_N	F35
17	GND		18	GND	
19	131_RX1_P	F39	20	131_TX1_P	G36
21	131_RX1_N	F40	22	131_TX1_N	G37
23	GND		24	GND	
25	131_RX0_P	G41	26	131_TX0_P	H34
27	131_RX0_N	G42	28	131_TX0_N	H35
29	GND		30	GND	
31	130_CLK0_P	R32	32	130_CLK1_P	N32
33	130_CLK0_N	R33	34	130_CLK1_N	N33
35	GND		36	GND	
37	130_RX3_P	H39	38	130_TX3_P	J36
39	130_RX3_N	H40	40	130_TX3_N	J37
41	GND		42	GND	
43	130_RX2_P	J41	44	130_TX2_P	K34
45	130_RX2_N	J42	46	130_TX2_N	K35
47	GND		48	GND	
49	130_RX1_P	K39	50	130_TX1_P	L36
51	130_RX1_N	K40	52	130_TX1_N	L37
53	GND		54	GND	
55	130_RX0_P	L41	56	130_TX0_P	M34
57	130_RX0_N	L42	58	130_TX0_N	M35
59	GND		60	GND	
61	129_CLK0_P	W32	62	129_CLK1_P	U32

63	129_CLK0_N	W33	64	129_CLK1_N	U33
65	GND		66	GND	
67	129_RX3_P	M39	68	129_TX3_P	N36
69	129_RX3_N	M40	70	129_TX3_N	N37
71	GND		72	GND	
73	129_RX2_P	N41	74	129_TX2_P	P34
75	129_RX2_N	N42	76	129_TX2_N	P35
77	GND		78	GND	
79	129_RX1_P	P39	80	129_TX1_P	R36
81	129_RX1_N	P40	82	129_TX1_N	R37
83	GND		84	GND	
85	129_RX0_P	R41	86	129_TX0_P	T34
87	129_RX0_N	R42	88	129_TX0_N	T35
89	GND		90	GND	
91	128_CLK0_P	AB34	92	128_CLK1_P	AA32
93	128_CLK0_N	AB35	94	128_CLK1_N	AA33
95	GND		96	GND	
97	128_RX3_P	T39	98	128_TX3_P	U36
99	128_RX3_N	T40	100	128_TX3_N	U37
101	GND		102	GND	
103	128_RX2_P	U41	104	128_TX2_P	V34
105	128_RX2_N	U42	106	128_TX2_N	V35
107	GND		108	GND	
109	128_RX1_P	V39	110	128_TX1_P	W36
111	128_RX1_N	V40	112	128_TX1_N	W37
113	GND		114	GND	
115	128_RX0_P	W41	116	128_TX0_P	Y34
117	128_RX0_N	W42	118	128_TX0_N	Y35
119	GND		120	GND	

Pin assignment of board to board connector J30

J30 is connected to the transceiver signal of BANK505 MGT, MIOs of PS.

The MIO level of PS is 1.8V standard

J30 Pin	Signal Name	Pin Number	J30 Pin	Signal Name	Pin Number
1	505_CLK2_N	AC38	2	505_CLK3_N	AA38

3	505_CLK2_P	AC37	4	505_CLK3_P	AA37
5	GND		6	GND	
7	505_TX3_N	AB40	8	505_RX3_N	AA42
9	505_TX3_P	AB39	10	505_RX3_P	AA41
11	GND		12	GND	
13	505_TX2_N	AD40	14	505_RX2_N	AC42
15	505_TX2_P	AD39	16	505_RX2_P	AC41
17	GND		18	GND	
19	505_TX1_N	AF40	20	505_RX1_N	AE42
21	505_TX1_P	AF39	22	505_RX1_P	AE41
23	GND		24	GND	
25	505_TX0_N	AH40	26	505_RX0_N	AG42
27	505_TX0_P	AH39	28	505_RX0_P	AG41
29	GND		30	GND	
31	505_CLK0_N	AG38	32	505_CLK1_N	AE38
33	505_CLK0_P	AG37	34	505_CLK1_P	AE37
35	GND		36	GND	
37	DP_HPD_MIO28	L28	38	DP_AUX_IN_MIO30	L30
39	DP_OE_MIO29	M27	40	DP_AUX_OUT_MIO27	L29
41	GND		42	GND	
43	PS_IIC1_SDA	AG34	44	USB_DIR	Y30
45	PS_IIC1_SCL	AH33	46	USB_CLK	W29
47	SD_CD	T29	48	USB_DATA5	AC32
49	SD_D1	T28	50	USB_DATA0	AA30
51	GND		52	GND	
53	SD_D2	V30	54	USB_DATA3	AC31
55	SD_D3	U29	56	USB_DATA2	Y29
57	SD_CLK	W30	58	USB_DATA6	AD31
59	SD_CMD	V29	60	USB_DATA1	AB30
61	GND		62	GND	
63	SD_D0	U28	64	USB_DATA7	AD30
65	悬空		66	USB_NXT	AB29
67	PS_MIO36	T27	68	USB_STP	AC29
69	PCIE_RSTN_MIO37	N30	70	USB_DATA4	AD29
71	GND		72	GND	
73	PS_UART_TX	P29	74	PHY1_RXD3	AG33

75	PS_UART_RX	R27	76	PHY1_RXCTL	AF33
77	PS_MIO42	T30	78	PHY1_RXD1	AF32
79	PS_MIO43	R30	80	PHY1_TXD3	AE33
81	GND		82	GND	
83	FPGA_DONE	Y28	84	PHY1_RXD0	AF31
85	PS_POR_B	W27	86	PHY1_TXCTL	AE32
87	VBAT_IN		88	PHY1_RXD2	AG30
89	PS_MIO44	R29	90	PHY1_RXCK	AF30
91	GND		92	GND	
93	CAN1_RX	P30	94	PHY1_TXD1	AD33
95	CAN1_TX	P28	96	PHY1_TXD2	AE30
97	CAN0_TX	N29	98	PHY1_TXD0	AE29
99	CAN0_RX	P27	100	PHY1_TXCK	AD32
101	GND		102	GND	
103	PS_UART2_RX	N28	104	PHY1_MDC	AH31
105	PS_UART2_TX	M30	106	PHY1_MDIO	AG31
107	PS_MIO31	M28	108	PCIE_PERSTN	AM25
109	PS_MIO26	L27	110	POWER_SW	
111	GND		112	GND	
113	PS_MODE2	AA28	114	PS_MODE3	AB28
115	PS_MODE0	AA27	116	PS_MODE1	AC28
117	FPGA_TDO	AD27	118	FPGA_TMS	AD26
119	FPGA_TCK	AC26	120	FPGA_TDI	AD25

Pin assignment of board to board connector J31

J31 connects the IO of BANK64, BANK65; the maximum voltage standard of BANK64, 65 is 1.8V(BANK power is supplied by carrier board).

J31 Pin	Signal Name	Pin Number	J31 Pin	Signal Name	Pin Number
1	B65_L10_N	AV28	2	B65_L18_N	AT28
3	B65_L10_P	AU28	4	B65_L18_P	AR28
5	B65_L16_N	AP27	6	B65_L15_N	AN26
7	B65_L16_P	AN27	8	B65_L15_P	AM26
9	GND		10	GND	
11	B65_L13_N	AT27	12	B65_L9_N	AW27
13	B65_L13_P	AR27	14	B65_L9_P	AV27

15	B65_L5_N	AY28	16	B65_L12_N	AT26
17	B65_L5_P	AY27	18	B65_L12_P	AT25
19	GND		20	GND	
21	B65_L8_N	AW26	22	B65_L11_N	AU26
23	B65_L8_P	AV26	24	B65_L11_P	AU25
25	B65_L20_N	AP25	26	B65_L6_N	BB28
27	B65_L20_P	AP24	28	B65_L6_P	BA28
29	GND		30	GND	
31	B65_L4_N	BB26	32	B65_L14_N	AR25
33	B65_L4_P	BA26	34	B65_L14_P	AR24
35	B65_L2_N	BB25	36	B65_L3_N	BA25
37	B65_L2_P	BB24	38	B65_L3_P	AY25
39	GND		40	GND	
41	B65_L7_N	AV24	42	B65_L1_N	AY24
43	B65_L7_P	AU24	44	B65_L1_P	AW24
45	B65_L21_N	AN24	46	B65_L22_N	AN23
47	B65_L21_P	AM24	48	B65_L22_P	AM23
49	GND		50	GND	
51	B65_L19_N	AT23	52	B65_L23_N	AL23
53	B65_L19_P	AR23	54	B65_L23_P	AK23
55	B65_L24_N	AK24	56	B65_L17_N	AN28
57	B65_L24_P	AJ24	58	B65_L17_P	AM28
59	GND		60	GND	
61	B64_L23_P	AJ21	62	B64_L1_P	BA23
63	B64_L23_N	AJ20	64	B64_L1_N	BB23
65	B64_L24_P	AJ22	66	B64_L16_P	AN21
67	B64_L24_N	AK22	68	B64_L16_N	AP21
69	GND		70	GND	
71	B64_L7_P	AU23	72	B64_L22_P	AK20
73	B64_L7_N	AV23	74	B64_L22_N	AK19
75	B64_L2_P	AY23	76	B64_L19_P	AM19
77	B64_L2_N	AY22	78	B64_L19_N	AN19
79	GND		80	GND	
81	B64_L20_P	AM21	82	B64_L14_P	AT20
83	B64_L20_N	AM20	84	B64_L14_N	AU19
85	B64_L11_P	AU21	86	B64_L3_P	BA22

87	B64_L11_N	AV21	88	B64_L3_N	BA21
89	GND		90	GND	
91	B64_L18_P	AP19	92	B64_L5_P	BB20
93	B64_L18_N	AR19	94	B64_L5_N	BB19
95	B64_L8_P	AV22	96	B64_L6_P	BA18
97	B64_L8_N	AW22	98	B64_L6_N	BB18
99	GND		100	GND	
101	B64_L21_P	AL22	102	B64_L9_P	AW20
103	B64_L21_N	AL21	104	B64_L9_N	AW19
105	B64_L15_P	AN22	106	B64_L10_P	AY19
107	B64_L15_N	AP22	108	B64_L10_N	AY18
109	GND		110	GND	
111	B64_L13_P	AT22	112	B64_L4_P	AY20
113	B64_L13_N	AT21	114	B64_L4_N	BA20
115	B64_L17_P	AP20	116	B64_L12_P	AU20
117	B64_L17_N	AR20	118	B64_L12_N	AV19
1	B65_L10_N	AV28	2	B65_L18_N	AT28

Pin assignment of board to board connector J32

J32 connects the IO of BANK66, 67; the maximum voltage standard of BANK66, 67 is 1.8V(BANK power is supplied by carrier board).

J32 Pin	Signal Name	Pin Number	J32 Pin	Signal Name	Pin Number
1	B66_L3_P	AW17	2	B66_L4_P	BA15
3	B66_L3_N	AW16	4	B66_L4_N	BB15
5	B66_L1_P	AY17	6	B66_L15_P	AU18
7	B66_L1_N	BA17	8	B66_L15_N	AV18
9	GND		10	GND	
11	B66_L13_P	AV17	12	B66_L16_P	AR18
13	B66_L13_N	AV16	14	B66_L16_N	AT18
15	B66_L17_P	AR17	16	B66_L2_P	BA16
17	B66_L17_N	AT17	18	B66_L2_N	BB16
19	GND		20	GND	
21	B66_L5_P	AY15	22	B66_L20_P	AL18
23	B66_L5_N	AY14	24	B66_L20_N	AM18
25	B66_L19_P	AJ18	26	B66_L21_P	AN18

27	B66_L19_N	AK18	28	B66_L21_N	AN17
29	GND		30	GND	
31	B66_L11_P	AW15	32	B66_L14_P	AT15
33	B66_L11_N	AW14	34	B66_L14_N	AU15
35	B66_L24_P	AN16	36	B66_L18_P	AT16
37	B66_L24_N	AP16	38	B66_L18_N	AU16
39	GND		40	GND	
41	B66_L22_P	AJ17	42	B66_L23_P	AL16
43	B66_L22_N	AK17	44	B66_L23_N	AM16
45	B66_L10_P	AU13	46	B66_L12_P	AU14
47	B66_L10_N	AV13	48	B66_L12_N	AV14
49	GND		50	GND	
51	B66_L7_P	AY12	52	B66_L9_P	BA10
53	B66_L7_N	BA12	54	B66_L9_N	BB10
55	B66_L8_P	BA11	56	B66_L6_P	BA13
57	B66_L8_N	BB11	58	B66_L6_N	BB13
59	GND		60	GND	
61	B67_L23_P	AM13	62	B67_L15_P	AR15
63	B67_L23_N	AN13	64	B67_L15_N	AR14
65	B67_L12_P	AT11	66	B67_L7_P	AV12
67	B67_L12_N	AT10	68	B67_L7_N	AW12
69	GND		70	GND	
71	B67_L16_P	AN12	72	B67_L11_P	AT13
73	B67_L16_N	AP12	74	B67_L11_N	AT12
75	B67_L14_P	AP10	76	B67_L13_P	AR13
77	B67_L14_N	AR10	78	B67_L13_N	AR12
79	GND		80	GND	
81	B67_L9_P	AW11	82	B67_L24_P	AJ14
83	B67_L9_N	AW10	84	B67_L24_N	AK14
85	B67_L3_P	AW8	86	B67_L22_P	AN14
87	B67_L3_N	AY8	88	B67_L22_N	AP14
89	GND		90	GND	
91	B67_L1_P	AW9	92	B67_L19_P	AL15
93	B67_L1_N	AY9	94	B67_L19_N	AM15
95	B67_L20_P	AJ15	96	B67_L17_P	AM11
97	B67_L20_N	AK15	98	B67_L17_N	AN11

99	GND		100	GND	
101	B67_L4_P	BA8	102	B67_L21_P	AL14
103	B67_L4_N	BA7	104	B67_L21_N	AM14
105	B67_L10_P	AV9	106	B67_L8_P	AU11
107	B67_L10_N	AV8	108	B67_L8_N	AV11
109	GND		110	GND	
111	B67_L2_P	BB9	112	B67_L5_P	BA6
113	B67_L2_N	BB8	114	B67_L5_N	BB6
115	B67_L6_P	BB5	116	B67_L18_P	AM10
117	B67_L6_N	BB4	118	B67_L18_N	AN10
119	GND		120	GND	

Pin assignment of board to board connector J33

J33 connects the GTH signal of BANK224,225,226,227.

J33 Pin	Signal Name	Pin Number	J33 Pin	Signal Name	Pin Number
1	224_TX0_N	AY3	2	224_RX0_N	BA1
3	224_TX0_P	AY4	4	224_RX0_P	BA2
5	GND		6	GND	
7	224_TX1_N	AW5	8	224_RX1_N	AW1
9	224_TX1_P	AW6	10	224_RX1_P	AW2
11	GND		12	GND	
13	224_TX2_N	AU5	14	224_RX2_N	AV3
15	224_TX2_P	AU6	16	224_RX2_P	AV4
17	GND		18	GND	
19	224_TX3_N	AT7	20	224_RX3_N	AU1
21	224_TX3_P	AT8	22	224_RX3_P	AU2
23	GND		24	GND	
25	224_CLK0_N	AK11	26	224_CLK1_N	AJ9
27	224_CLK0_P	AK12	28	224_CLK1_P	AJ10
29	GND		30	GND	
31	225_TX0_N	AR5	32	225_RX0_N	AT3
33	225_TX0_P	AR6	34	225_RX0_P	AT4
35	GND		36	GND	
37	225_TX1_N	AP7	38	225_RX1_N	AR1
39	225_TX1_P	AP8	40	225_RX1_P	AR2

41	GND		42	GND	
43	225_TX2_N	AN5	44	225_RX2_N	AP3
45	225_TX2_P	AN6	46	225_RX2_P	AP4
47	GND		48	GND	
49	225_TX3_N	AM7	50	225_RX3_N	AN1
51	225_TX3_P	AM8	52	225_RX3_P	AN2
53	GND		54	GND	
55	225_CLK0_N	AH11	56	225_CLK1_N	AG9
57	225_CLK0_P	AH12	58	225_CLK1_P	AG10
59	GND		60	GND	
61	226_TX0_N	AL5	62	226_RX0_N	AM3
63	226_TX0_P	AL6	64	226_RX0_P	AM4
65	GND		66	GND	
67	226_TX1_N	AK7	68	226_RX1_N	AL1
69	226_TX1_P	AK8	70	226_RX1_P	AL2
71	GND		72	GND	
73	226_TX2_N	AJ5	74	226_RX2_N	AK3
75	226_TX2_P	AJ6	76	226_RX2_P	AK4
77	GND		78	GND	
79	226_TX3_N	AH7	80	226_RX3_N	AJ1
81	226_TX3_P	AH8	82	226_RX3_P	AJ2
83	GND		84	GND	
85	226_CLK0_N	AF11	86	226_CLK1_N	AE9
87	226_CLK0_P	AF12	88	226_CLK1_P	AE10
89	GND		90	GND	
91	227_TX0_N	AG5	92	227_RX0_N	AH3
93	227_TX0_P	AG6	94	227_RX0_P	AH4
95	GND		96	GND	
97	227_TX1_N	AF7	98	227_RX1_N	AG1
99	227_TX1_P	AF8	100	227_RX1_P	AG2
101	GND		102	GND	
103	227_TX2_N	AE5	104	227_RX2_N	AF3
105	227_TX2_P	AE6	106	227_RX2_P	AF4
107	GND		108	GND	
109	227_TX3_N	AD7	110	227_RX3_N	AE1
111	227_TX3_P	AD8	112	227_RX3_P	AE2

113	GND		114	GND	
115	227_CLK0_N	AD11	116	227_CLK1_N	AC9
117	227_CLK0_P	AD12	118	227_CLK1_P	AC10
119	GND		120	GND	

Pin assignment of board to board connector J34

J34 connects the GTH signal of BANK228,229,230,231.

J34 Pin	Signal Name	Pin Number	J34 Pin	Signal Name	Pin Number
1	228_TX0_N	AC5	2	228_RX0_N	AD3
3	228_TX0_P	AC6	4	228_RX0_P	AD4
5	GND		6	GND	
7	228_TX1_N	AB7	8	228_RX1_N	AC1
9	228_TX1_P	AB8	10	228_RX1_P	AC2
11	GND		12	GND	
13	228_TX2_N	AA5	14	228_RX2_N	AB3
15	228_TX2_P	AA6	16	228_RX2_P	AB4
17	GND		18	GND	
19	228_TX3_N	Y7	20	228_RX3_N	AA1
21	228_TX3_P	Y8	22	228_RX3_P	AA2
23	GND		24	GND	
25	228_CLK1_N	AA9	26	228_CLK0_N	AB11
27	228_CLK1_P	AA10	28	228_CLK0_P	AB12
29	GND		30	GND	
31	229_TX0_N	W5	32	229_RX0_N	Y3
33	229_TX0_P	W6	34	229_RX0_P	Y4
35	GND		36	GND	
37	229_TX1_N	V7	38	229_RX1_N	W1
39	229_TX1_P	V8	40	229_RX1_P	W2
41	GND		42	GND	
43	229_TX2_N	U5	44	229_RX2_N	V3
45	229_TX2_P	U6	46	229_RX2_P	V4
47	GND		48	GND	
49	229_TX3_N	T7	50	229_RX3_N	U1
51	229_TX3_P	T8	52	229_RX3_P	U2
53	GND		54	GND	

55	229_CLK1_N	W9	56	229_CLK0_N	Y11
57	229_CLK1_P	W10	58	229_CLK0_P	Y12
59	GND		60	GND	
61	230_TX0_N	R5	62	230_RX0_N	T3
63	230_TX0_P	R6	64	230_RX0_P	T4
65	GND		66	GND	
67	230_TX1_N	P7	68	230_RX1_N	R1
69	230_TX1_P	P8	70	230_RX1_P	R2
71	GND		72	GND	
73	230_TX2_N	N5	74	230_RX2_N	P3
75	230_TX2_P	N6	76	230_RX2_P	P4
77	GND		78	GND	
79	230_TX3_N	M7	80	230_RX3_N	N1
81	230_TX3_P	M8	82	230_RX3_P	N2
83	GND		84	GND	
85	230_CLK1_N	U9	86	230_CLK0_N	V11
87	230_CLK1_P	U10	88	230_CLK0_P	V12
89	GND		90	GND	
91	231_TX0_N	L5	92	231_RX0_N	M3
93	231_TX0_P	L6	94	231_RX0_P	M4
95	GND		96	GND	
97	231_TX1_N	K3	98	231_RX1_N	L1
99	231_TX1_P	K4	100	231_RX1_P	L2
101	GND		102	GND	
103	231_TX2_N	J5	104	231_RX2_N	J1
105	231_TX2_P	J6	106	231_RX2_P	J2
107	GND		108	GND	AC20
109	231_TX3_N	H3	110	231_RX3_N	G1
111	231_TX3_P	H4	112	231_RX3_P	G2
113	GND		114	GND	
115	231_CLK1_N	R9	116	231_CLK0_N	T11
117	231_CLK1_P	R10	118	231_CLK0_P	T12
119	GND		120	GND	

Pin assignment of board to board connector J35

J35 connects power supply of +12V and the IOs of BANK91,93,94; the

voltage standard is 3.3V.

J35 Pin	Signal Name	Pin Number	J35 Pin	Signal Name	Pin Number
1	+12V		2	GND	
3	+12V		4	GND	
5	+12V		6	GND	
7	+12V		8	GND	
9	+12V		10	GND	
11	+12V		12	GND	
13	+12V		14	GND	
15	+12V		16	GND	
17	+12V		18	GND	
19	+12V		20	GND	
21	+12V		22	GND	
23	+12V		24	GND	
25	+12V		26	GND	
27	+12V		28	GND	
29	+12V		30	GND	
31	GND		32	GND	
33	B94_L5_N	D3	34	B94_L8_N	C3
35	B94_L5_P	D4	36	B94_L8_P	C4
37	B94_L7_N	C5	38	B94_L12_N	A4
39	B94_L7_P	C6	40	B94_L12_P	A5
41	GND		42	GND	
43	B94_L3_N	E2	44	B94_L4_N	D1
45	B94_L3_P	E3	46	B94_L4_P	E1
47	B94_L6_N	C1	48	B94_L9_N	B1
49	B94_L6_P	D2	50	B94_L9_P	B2
51	GND		52	GND	
53	B94_L1_N	F4	54	B94_L11_N	B5
55	B94_L1_P	F5	56	B94_L11_P	B6
57	B94_L10_N	A3	58	B94_L2_N	E4
59	B94_L10_P	B3	60	B94_L2_P	E5
61	GND		62	GND	
63	B93_L10_N	A7	64	B93_L1_N	F6
65	B93_L10_P	B7	66	B93_L1_P	G6
67	B93_L9_N	D6	68	B93_L5_N	F7

69	B93_L9_P	E6	70	B93_L5_P	G7
71	GND		72	GND	
73	B93_L7_N	D7	74	B93_L2_N	H8
75	B93_L7_P	E7	76	B93_L2_P	J8
77	B93_L8_N	C8	78	B93_L4_N	E9
79	B93_L8_P	D8	80	B93_L4_P	F9
81	GND		82	GND	
83	B93_L3_N	H9	84	B93_L6_N	F8
85	B93_L3_P	J9	86	B93_L6_P	G8
87	B93_L11_N	A8	88	B93_L12_N	C9
89	B93_L11_P	B8	90	B93_L12_P	D9
91	GND		92	GND	
93	B91_L12_N	A9	94	B91_L7_N	E10
95	B91_L12_P	A10	96	B91_L7_P	E11
97	B91_L5_N	F10	98	B91_L1_N	H10
99	B91_L5_P	G10	100	B91_L1_P	J11
101	GND		102	GND	
103	B91_L10_N	B10	104	B91_L9_N	C11
105	B91_L10_P	C10	106	B91_L9_P	D11
107	B91_L11_N	B11	108	B91_L2_N	G11
109	B91_L11_P	B12	110	B91_L2_P	H11
111	GND		112	GND	
113	B91_L3_N	G12	114	B91_L8_N	D12
115	B91_L3_P	H13	116	B91_L8_P	E12
117	B91_L4_N	G13	118	B91_L6_N	F12
119	B91_L4_P	H14	120	B91_L6_P	F13

Pin assignment of board to board connector J36

J35 connects BANK power supply of VCCIO64~68,the IOs of BANK68,90; the maximum voltage standard of BANK68 is 1.8V, voltage standard of BANK90 is 3.3V

J36 Pin	Signal Name	Pin Number	J36 Pin	Signal Name	Pin Number
1	VCCO_68		2	B68_L16_N	A12
3	VCCO_68		4	B68_L16_P	B13
5	GND		6	B68_L17_N	A13

7	GND		8	B68_L17_P	A14
9	VCCO_67		10	GND	
11	VCCO_67		12	B68_L15_N	C13
13	GND		14	B68_L15_P	D13
15	GND		16	B68_L1_N	N15
17	VCCO_66		18	B68_L1_P	P15
19	VCCO_66		20	GND	
21	GND		22	B68_L14_N	D14
23	GND		24	B68_L14_P	E15
25	VCCO_64		26	B68_L13_N	E14
27	VCCO_64		28	B68_L13_P	F14
29	GND		30	GND	
31	GND		32	B68_L18_N	B15
33	VCCO_65		34	B68_L18_P	C15
35	VCCO_65		36	B68_L12_N	F15
37	GND		38	B68_L12_P	G16
39	GND		40	GND	
41	-		42	B68_L20_N	B16
43	-		44	B68_L20_P	C16
45	-		46	B68_L19_N	D16
47	-		48	B68_L19_P	E16
49	GND		50	GND	
51	-		52	B68_L22_N	A17
53	-		54	B68_L22_P	B17
55	-		56	B68_L21_N	D17
57	-		58	B68_L21_P	E17
59	GND		60	GND	
61	B90_L12_N	J12	62	B68_L24_N	A18
63	B90_L12_P	J13	64	B68_L24_P	B18
65	B90_L7_N	K12	66	B68_L23_N	C18
67	B90_L7_P	L12	68	B68_L23_P	D18
69	GND		70	GND	
71	B90_L10_N	K10	72	B68_L7_N	G15
73	B90_L10_P	K11	74	B68_L7_P	H15
75	B90_L8_N	L13	76	B68_L5_N	K15
77	B90_L8_P	L14	78	B68_L5_P	K16

79	GND		80	GND	
81	B90_L11_N	J14	82	B68_L11_N	F17
83	B90_L11_P	K14	84	B68_L11_P	G17
85	B90_L5_N	M13	86	B68_L10_N	F18
87	B90_L5_P	N13	88	B68_L10_P	G18
89	GND		90	GND	
91	B90_L4_N	N14	92	B68_L8_N	H16
93	B90_L4_P	P14	94	B68_L8_P	J16
95	B90_L3_N	P13	96	B68_L6_N	K17
97	B90_L3_P	R14	98	B68_L6_P	L17
99	GND		100	GND	
101	B90_L2_N	N12	102	B68_L9_N	H18
103	B90_L2_P	P12	104	B68_L9_P	J18
105	B90_L9_N	L10	106	B68_L3_N	M16
107	B90_L9_P	M10	108	B68_L3_P	M17
109	GND		110	GND	
111	B90_L6_N	M11	112	B68_L4_N	L15
113	B90_L6_P	M12	114	B68_L4_P	M15
115	B90_L1_N	N10	116	B68_L2_N	N16
117	B90_L1_P	N11	118	B68_L2_P	P16
119	GND		120	GND	

Part 3: Carrier Board

Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- PCEI3.0 x16 interface
- M.2 interface
- DP output interface
- USB 3.0 Interfaces
- 2-Channel 10/100M/1000M Ethernet RJ-45 interface
- 2-Channel USB Uart Interfaces
- Micro TF card slot
- 2-Channel FMC HPC interface
- JTAG debugging interface
- 1-Channel temperature sensor
- 1-Channel EEPROM
- 2 LED lights

Part 3.2: PCIE3.0 X16 Interface

The Z19-P development board has a PCIE 3.0 x16 endpoint interface for PCIE communication. 16 pairs GTH signals of BANK224,225,226,227 are connected to PCIE slot, each lane of PCIE can reach 8Gbps speed, which can realize PCIE 3.0 (compatible 2.0) data communication.

The PCIe interface is shown in Figure 3-2-1 below, where the TX signal is connected in AC coupling mode.

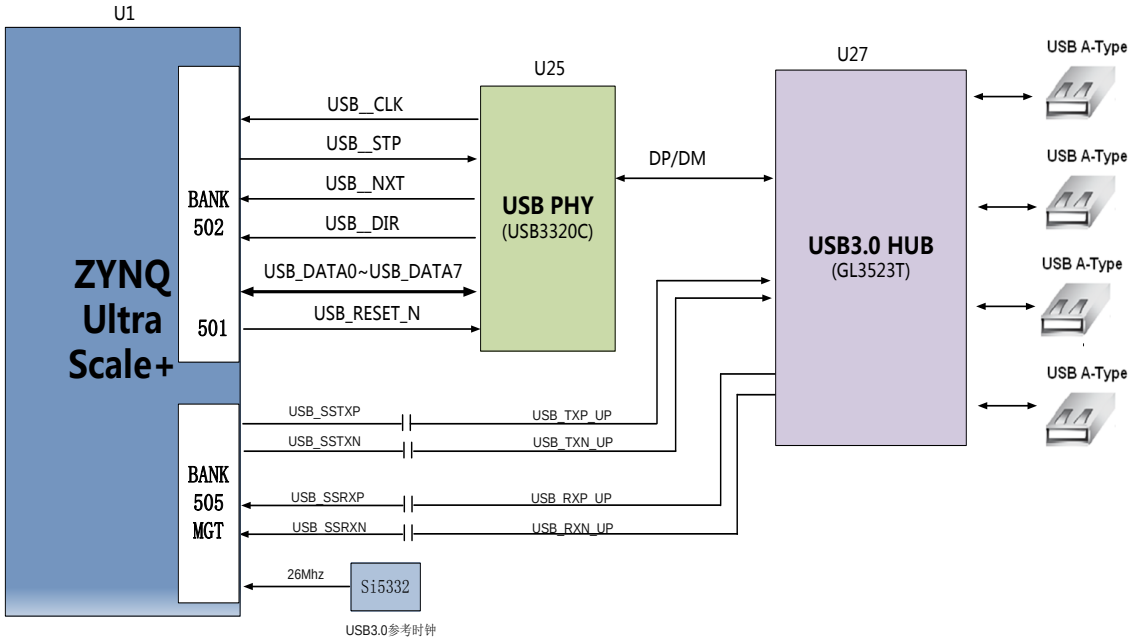


Figure 3-2-1: PCIe Interface Schematic

PCIe x16 Interface ZYNQ Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PCIE_CLK_N	225_CLK0_N	AH11	PCIE Channel reference clock Negative
PCIE_CLK_P	225_CLK0_P	AH12	PCIE Channel reference clock Positive
PCIE_RX15_N	224_RX0_N	BA1	PCIE Channel 15 Data Receive Negative
PCIE_RX15_P	224_RX0_P	BA2	PCIE Channel 15 Data Receive Positive
PCIE_RX14_N	224_RX1_N	AW1	PCIE Channel 14 Data Receive Negative
PCIE_RX14_P	224_RX1_P	AW2	PCIE Channel 14 Data Receive Positive
PCIE_RX13_N	224_RX2_N	AV3	PCIE Channel 13 Data Receive Negative
PCIE_RX13_P	224_RX2_P	AV4	PCIE Channel 13 Data Receive Positive
PCIE_RX12_N	224_RX3_N	AU1	PCIE Channel 12 Data Receive Negative
PCIE_RX12_P	224_RX3_P	AU2	PCIE Channel 12 Data Receive Positive
PCIE_RX11_N	225_RX0_N	AT3	PCIE Channel 11 Data Receive Negative
PCIE_RX11_P	225_RX0_P	AT4	PCIE Channel 11 Data Receive Positive
PCIE_RX10_N	225_RX1_N	AR1	PCIE Channel 10 Data Receive Negative
PCIE_RX10_P	225_RX1_P	AR2	PCIE Channel 10 Data Receive Positive
PCIE_RX9_N	225_RX2_N	AP3	PCIE Channel 9 Data Receive Negative
PCIE_RX9_P	225_RX2_P	AP4	PCIE Channel 9 Data Receive Positive
PCIE_RX8_N	225_RX3_N	AN1	PCIE Channel 8 Data Receive Negative

PCIE_RX8_P	225_RX3_P	AN2	PCIE Channel 8 Data Receive Positive
PCIE_RX7_N	226_RX0_N	AM3	PCIE Channel 7 Data Receive Negative
PCIE_RX7_P	226_RX0_P	AM4	PCIE Channel 7 Data Receive Positive
PCIE_RX6_N	226_RX1_N	AL1	PCIE Channel 6 Data Receive Negative
PCIE_RX6_P	226_RX1_P	AL2	PCIE Channel 6 Data Receive Positive
PCIE_RX5_N	226_RX2_N	AK3	PCIE Channel 5 Data Receive Negative
PCIE_RX5_P	226_RX2_P	AK4	PCIE Channel 5 Data Receive Positive
PCIE_RX4_N	226_RX3_N	AJ1	PCIE Channel 4 Data Receive Negative
PCIE_RX4_P	226_RX3_P	AJ2	PCIE Channel 4 Data Receive Positive
PCIE_RX3_N	227_RX0_N	AH3	PCIE Channel 3 Data Receive Negative
PCIE_RX3_P	227_RX0_P	AH4	PCIE Channel 3 Data Receive Positive
PCIE_RX2_N	227_RX1_N	AG1	PCIE Channel 2 Data Receive Negative
PCIE_RX2_P	227_RX1_P	AG2	PCIE Channel 2 Data Receive Positive
PCIE_RX1_N	227_RX2_N	AF3	PCIE Channel 1 Data Receive Negative
PCIE_RX1_P	227_RX2_P	AF4	PCIE Channel 1 Data Receive Positive
PCIE_RX0_N	227_RX3_N	AE1	PCIE Channel 0 Data Receive Negative
PCIE_RX0_P	227_RX3_P	AE2	PCIE Channel 0 Data Receive Positive
PCIE_TX15_N	224_TX0_N	AY3	PCIE Channel 15 Data Transmit Negative
PCIE_TX15_P	224_TX0_P	AY4	PCIE Channel 15 Data Transmit Positive
PCIE_TX14_N	224_TX1_N	AW5	PCIE Channel 14 Data Transmit Negative
PCIE_TX14_P	224_TX1_P	AW6	PCIE Channel 14 Data Transmit Positive
PCIE_TX13_N	224_TX2_N	AU5	PCIE Channel 13 Data Transmit Negative
PCIE_TX13_P	224_TX2_P	AU6	PCIE Channel 13 Data Transmit Positive
PCIE_TX12_N	224_TX3_N	AT7	PCIE Channel 12 Data Transmit Negative
PCIE_TX12_P	224_TX3_P	AT8	PCIE Channel 12 Data Transmit Positive
PCIE_TX11_N	225_TX0_N	AR5	PCIE Channel 11 Data Transmit Negative
PCIE_TX11_P	225_TX0_P	AR6	PCIE Channel 11 Data Transmit Positive
PCIE_TX10_N	225_TX1_N	AP7	PCIE Channel 10 Data Transmit Negative
PCIE_TX10_P	225_TX1_P	AP8	PCIE Channel 10 Data Transmit Positive
PCIE_TX9_N	225_TX2_N	AN5	PCIE Channel 9 Data Transmit Negative
PCIE_TX9_P	225_TX2_P	AN6	PCIE Channel 9 Data Transmit Positive
PCIE_TX8_N	225_TX3_N	AM7	PCIE Channel 8 Data Transmit Negative
PCIE_TX8_P	225_TX3_P	AM8	PCIE Channel 8 Data Transmit Positive
PCIE_TX7_N	226_TX0_N	AL5	PCIE Channel 7 Data Transmit Negative
PCIE_TX7_P	226_TX0_P	AL6	PCIE Channel 7 Data Transmit Positive
PCIE_TX6_N	226_TX1_N	AK7	PCIE Channel 6 Data Transmit Negative

PCIE_TX6_P	226_TX1_P	AK8	PCIE Channel 6 Data Transmit Positive
PCIE_TX5_N	226_TX2_N	AJ5	PCIE Channel 5 Data Transmit Negative
PCIE_TX5_P	226_TX2_P	AJ6	PCIE Channel 5 Data Transmit Positive
PCIE_TX4_N	226_TX3_N	AH7	PCIE Channel 4 Data Transmit Negative
PCIE_TX4_P	226_TX3_P	AH8	PCIE Channel 4 Data Transmit Positive
PCIE_TX3_N	227_TX0_N	AG5	PCIE Channel 3 Data Transmit Negative
PCIE_TX3_P	227_TX0_P	AG6	PCIE Channel 3 Data Transmit Positive
PCIE_TX2_N	227_TX1_N	AF7	PCIE Channel 2 Data Transmit Negative
PCIE_TX2_P	227_TX1_P	AF8	PCIE Channel 2 Data Transmit Positive
PCIE_TX1_N	227_TX2_N	AE5	PCIE Channel 1 Data Transmit Negative
PCIE_TX1_P	227_TX2_P	AE6	PCIE Channel 1 Data Transmit Positive
PCIE_TX0_N	227_TX3_N	AD7	PCIE Channel 0 Data Transmit Negative
PCIE_TX0_P	227_TX3_P	AD8	PCIE Channel 0 Data Transmit Positive
PCIE_PERSTN	IO_T3U_PERSTN0_65	AM25	PCIE Board Reset Signal

Part 3.3: M.2 Interface

The Z19-P board is equipped M.2 interface for connecting M.2 SSD, it is a PCIEx1 standard and the communication speed of up to 6Gbps. The M.2 interface uses the M key slot, which only supports PCI-E, not SATA. When users choose SSD drives, they need to choose PCIE type SSD.

The PCIE signal is directly connected to the BANK505 PS MGT transceiver of ZU19EG, and the TX signal and RX signal of one channel are connected to the LANE1 of MGT in a differential signal mode. The PCIE reference clock is provided by the Si5332 chipset, the frequency is 100Mhz, and the schematic diagram of the M.2 circuit design is shown in Figure 3-3-1:

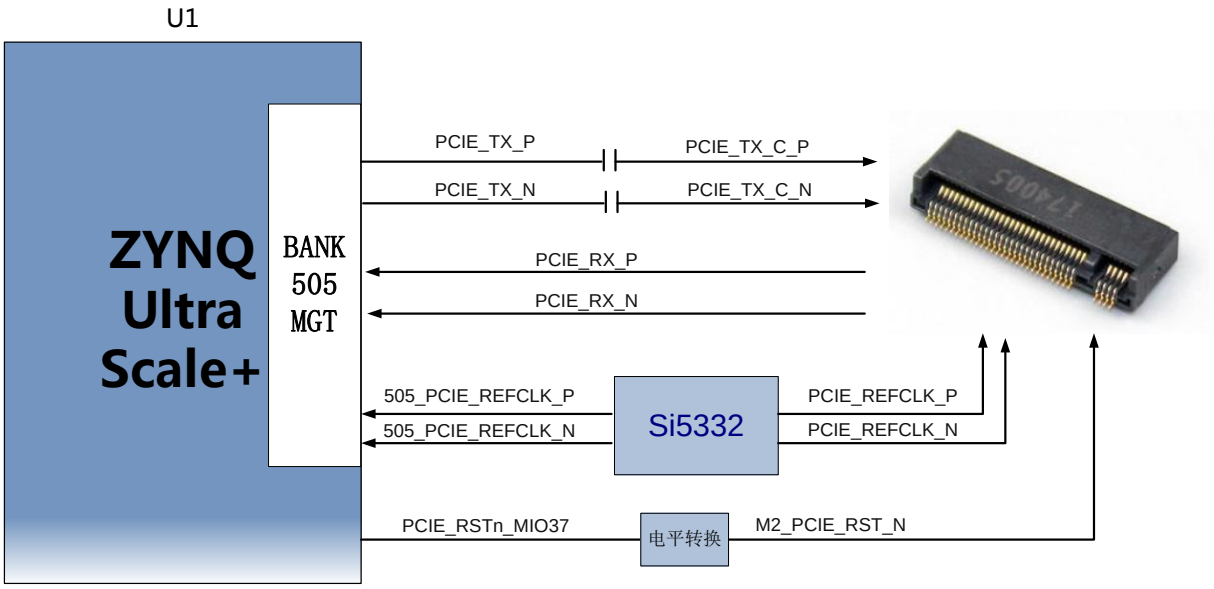


Figure 3-3-1: M.2 Interface Schematic

The pin assignment of M.2 interface ZYNQ is as follows:

Signal Name	Pin Name	Pin Number	Description
PCIE_TX_P	PS_MGTRTXP0_505	AH39	PCIE Data Transmit Positive
PCIE_TX_N	PS_MGTRTXN0_505	AH40	PCIE Data Transmit Negative
PCIE_RX_P	PS_MGTRRXP0_505	AG41	PCIE Data Receive Positive
PCIE_RX_N	PS_MGTRRXN0_505	AG42	PCIE Data Receive Negative
505_PCIE_REFCLK_P	PS_MGTREFCLK0P_505	AG37	PCIE Reference Clock Positive
505_PCIE_REFCLK_N	PS_MGTREFCLK0N_505	AG38	PCIE Reference Clock Negative
PCIE_RSTN_MIO37	PS_MIO37_501	N30	PCIE Reset Signal

Part 3.4: DP Interface

The Z19-P board has a MINI DP for video image display. The output supports VESA DP V1.2a output standard, up to 4K x 2K@30Fps output, supports Y-only, YCbCr444, YCbCr422, YCbCr420 and RGB video formats, each color supports 6, 8, 10, or 12 bits.

The DP data transmission channel is directly driven and output by the BANK505 PS MGT of ZU19EG, and the LANE2 and LANE3 TX signals of MGT are connected to the DP connector in a differential signal mode. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. The

schematic diagram of the DP output interface design is shown in Figure 3-4-1:

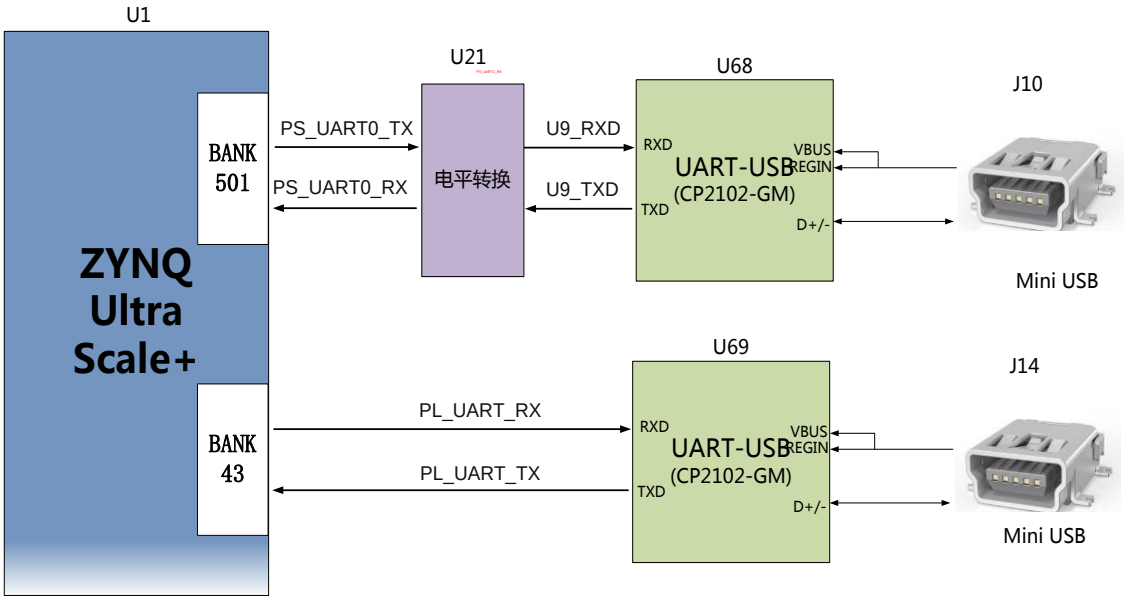


Figure 3-4-1: DP interface design Schematic

The DisplayPort interface ZYNQ pin assignment is as follows:

Signal Name	Pin Number	Pin Number	Description
GT0_DP_TX_P	PS_MGTRTXP3_505	AB39	Low bits of DP Data Transmit Positive
GT0_DP_TX_N	PS_MGTRTXN3_505	AB40	Low bits of DP Data Transmit Negative
GT1_DP_TX_P	PS_MGTRTXP2_505	AD39	High bits of DP Data Transmit Positive
GT1_DP_TX_N	PS_MGTRTXN2_505	AD40	High bits of DP Data Transmit Negative
505_DP_CLKP	PS_MGTREFCLK2P_505	AC37	DP Reference Clock Positive
505_DP_CLKN	PS_MGTREFCLK2N_505	AC38	DP Reference Clock Negative
DP_AUX_OUT_MIO27	PS_MIO27_501	L29	DP Auxiliary Data Output
DP_AUX_IN_MIO30	PS_MIO30_501	L30	DP Auxiliary Data Input
DP_OE_MIO29	PS_MIO29_501	M27	DP Auxiliary Data Output Enable
DP_HPD_MIO28	PS_MIO28_501	L28	DP Insertion Signal Detection

Part 3.5: USB3.0 Interface

There is a USB3.0 ports on the Z19-P carrier board, supporting the Host/OTG/Slave operation mode, and the data speed for USB3.0 is up to 5.0Gb/s. USB3.0 is connected through the PIPE3 interface, and USB2.0 is connected to the a USB3320C chipset through the ULPI interface to realize high-speed USB3.0 and USB2.0 data communication.

The USB connector is USB Type C, the schematic diagram of USB3.0 connection is shown as 3-5-1:

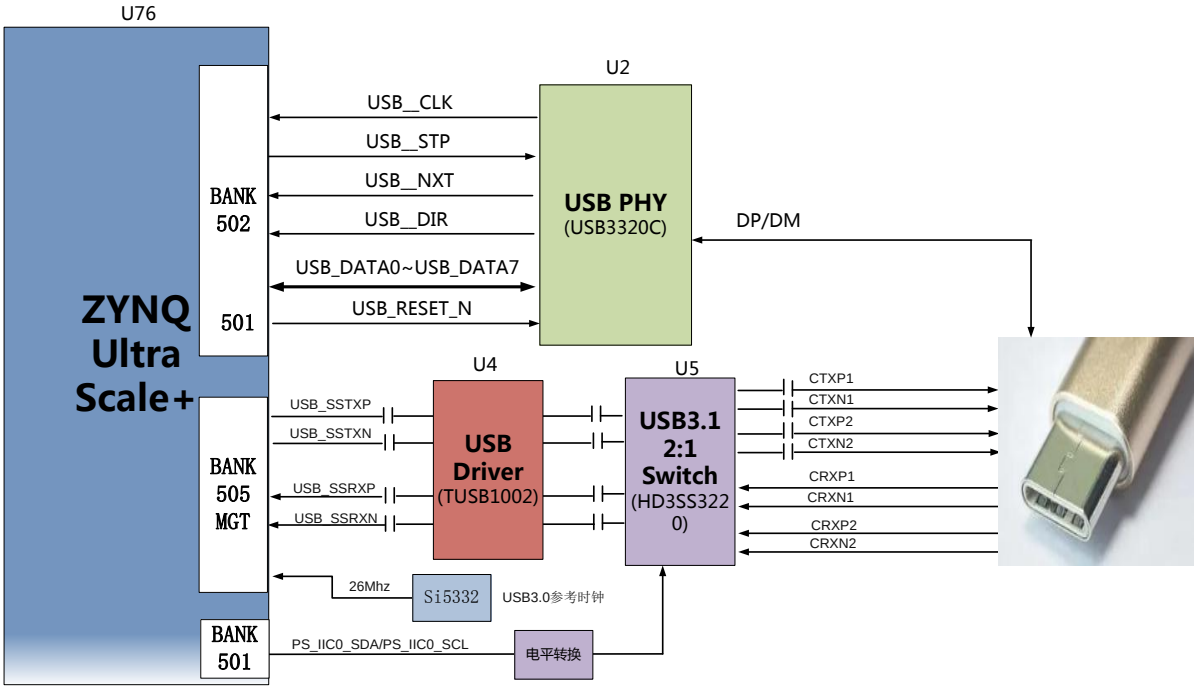


Figure 3-5-1: USB3.0 Interface Schematic

USB Interface Pin Assignment:

Signal Name	Pin Name	Pin Number	Description
USB_SSTXP	PS_MGTRTXP1_505	AF39	USB3.0 Data Transmit Positive
USB_SSTXN	PS_MGTRTXN1_505	AF40	USB3.0 Data Transmit Negative
USB_SSRXP	PS_MGTRRXP1_505	AE41	USB3.0 Data Receive Positive
USB_SSRXN	PS_MGTRRXN1_505	AE42	USB3.0 Data Receive Negative
USB_DATA0	PS_MIO56_502	AA30	USB2.0 Data Bit0
USB_DATA1	PS_MIO57_502	AB30	USB2.0 Data Bit1
USB_DATA2	PS_MIO54_502	Y29	USB2.0 Data Bit2
USB_DATA3	PS_MIO59_502	AC31	USB2.0 Data Bit3

USB_DATA4	PS_MIO60_502	AD29	USB2.0 Data Bit4
USB_DATA5	PS_MIO61_502	AC32	USB2.0 Data Bit5
USB_DATA6	PS_MIO62_502	AD31	USB2.0 Data Bit6
USB_DATA7	PS_MIO63_502	AD30	USB2.0 Data Bit7
USB_STP	PS_MIO58_502	AC29	USB2.0 Stop Signal
USB_DIR	PS_MIO53_502	Y30	USB2.0 Data Direction Signal
USB_CLK	PS_MIO52_502	W29	USB2.0 Clock Signal
USB_NXT	PS_MIO55_502	AB29	USB2.0 Next Data Signal
USB_RESET_N	PS_MIO44_501	R29	USB2.0 Reset Signal

Part 3.6: Gigabit Ethernet Interface

There is a Gigabit Ethernet ports on the Z19-P carrier board, which is connected to the PS MIOs. The GPHY chip is JL2121 Ethernet PHY chipset,it supports 10/100/1000 Mbps network communication.

When the JL2121 is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Table 3-6-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	MDIO/MDC Mode PHY Address	PHY Address 001
RXD1_TXDLY	TX Clock delay time 2ns	Delay time enable
RXD0_RXDLY	RX Clock delay time 2ns	Delay time enable

Table 3-6-1: PHY chip default configuration value

the schematic diagram of Gigabit Ethernet Interface is shown as 3-6-1:

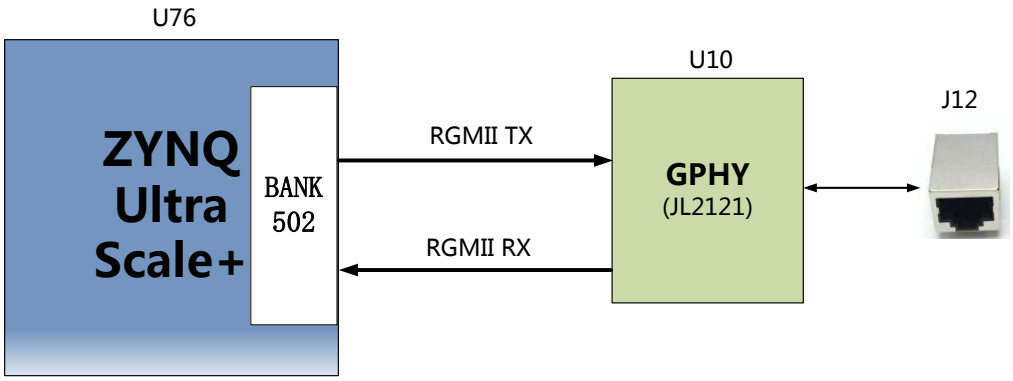


Figure 3-6-1: ZYNQ and GPHY connection diagram

PS Gigabit Ethernet pin assignment is as follows

Signal Name	Pin Name	Pin Number	Description
PHY1_TXCK	PHY1_TXCK	J31	Ethernet 1 RGMII Transmit Clock
PHY1_TXD0	PHY1_TXD0	J32	Ethernet 1 Transmit data bit0
PHY1_TXD1	PHY1_TXD1	J34	Ethernet 1 Transmit data bit1
PHY1_TXD2	PHY1_TXD2	K28	Ethernet 1 Transmit data bit2
PHY1_TXD3	PHY1_TXD3	K29	Ethernet 1 Transmit data bit3
PHY1_TXCTL	PHY1_TXCTL	K30	Ethernet 1 Transmit Enable Signal
PHY1_RXCK	PHY1_RXCK	K31	Ethernet 1 RGMII Receive Clock
PHY1_RXD0	PHY1_RXD0	K32	Ethernet 1 Receive Data Bit0
PHY1_RXD1	PHY1_RXD1	K33	Ethernet 1 Receive Data Bit1
PHY1_RXD2	PHY1_RXD2	K34	Ethernet 1 Receive Data Bit2
PHY1_RXD3	PHY1_RXD3	L29	Ethernet 1 Receive Data Bit3
PHY1_RXCTL	PHY1_RXCTL	L30	Ethernet 1 Receive Enable Signal
PHY1_MDC	PHY1_MDC	L33	Ethernet 1 MDIO Clock Management
PHY1_MDIO	PHY1_MDIO	L34	Ethernet 1 MDIO Management Data

Part 3.7: USB to Serial Port

The Z19-P carrier board has two Uart to USB ports, one is connected to the PS MIOs, and one is connected to the PL IOs.

The bridge of UART to USB is Silicon Labs CP2102GM's USB-UAR chipset, and the USB connector is a MINI USB port.

The schematic diagram of the USB Uart circuit design is shown in Figure

3-7-1:

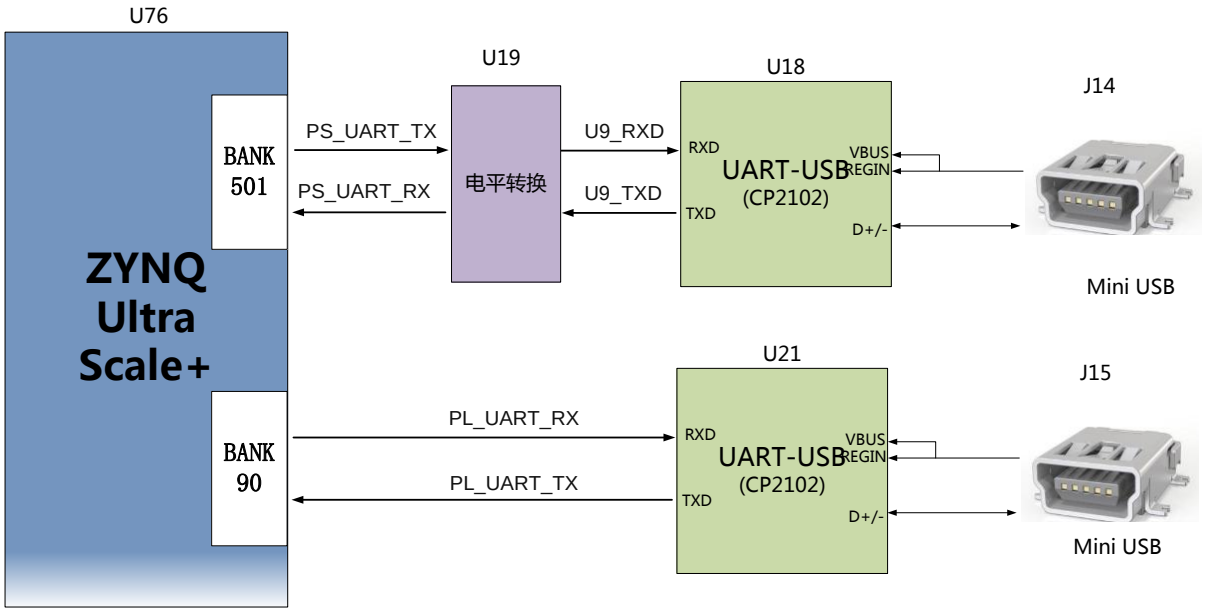


Figure 3-7-1: USB to serial port schematic

USB to serial port ZYNQ pin assignment:

Signal name	Pin Name	Pin Number	Description
PS_UART_RX	PS_MIO38	R27	PS Uart Data Input
PS_UART_TX	PS_MIO39	P29	PS Uart Data Output
PL_UART_RX	B90_L6_N	M11	PL Uart Data Input
PL_UART_TX	B90_L6_P	M12	PL Uart Data Output

Part 3.8: SD Card Slot Interface

The Z19-P Development Board contains a TF card slot for process to access the TF card memory, or BOOT program from TF card.

The design of the ZU19EG and TF card connector is shown in Figure 3-8-1:

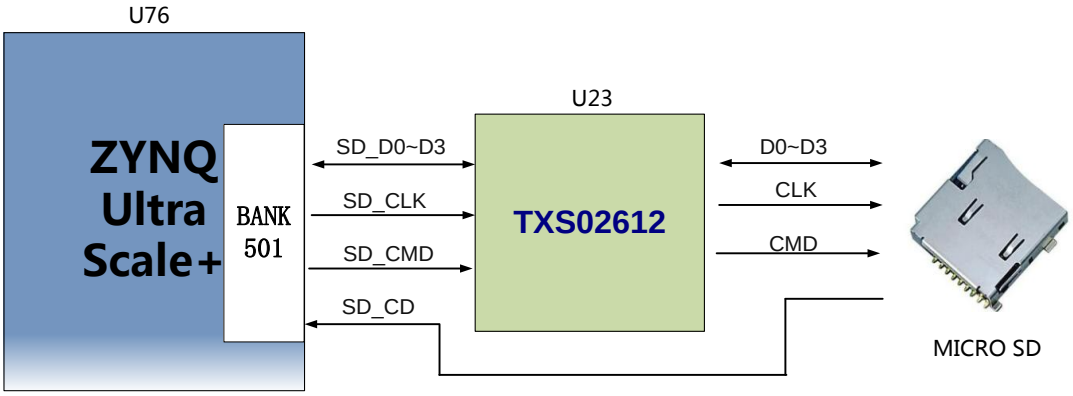


Figure 3-8-1: SD Card Connection Diagram

SD card slot pin assignment:

Signal Name	Pin Name	Pin Number	Description
SD_CMD	SD_CMD	P25	SD Clock Signal
SD_CD	SD_CD	P24	SD Command Signal
SD_D0	SD_D0	J25	SD Data0
SD_D1	SD_D1	L25	SD Data1
SD_D2	SD_D2	M25	SD Data2
SD_D3	SD_D3	K25	SD Data3
SD_CMD	SD_CMD	P25	SD card insertion signal

Part 3.9: FMC Interface

The Z19-P Carrier board has two standard FMC HPC interface that can be connected to FMC modules of XILINX or ALINX. In FMC1,it contains 72 pairs of differential IO signals and 8 pairs of GTX Transceivers. In FMC2it contains 42 pairs of differential IO signals and 8 pairs of GTX Transceivers,

The maximum voltage of FMC IO is 1.8V, the voltage can be changed to 1.2V by the jumper 2PIN connector(J23,J24).

The design diagram of ZYNQ Ultrascale+ and FMC1 connectors is shown in Figure 3-9-1.

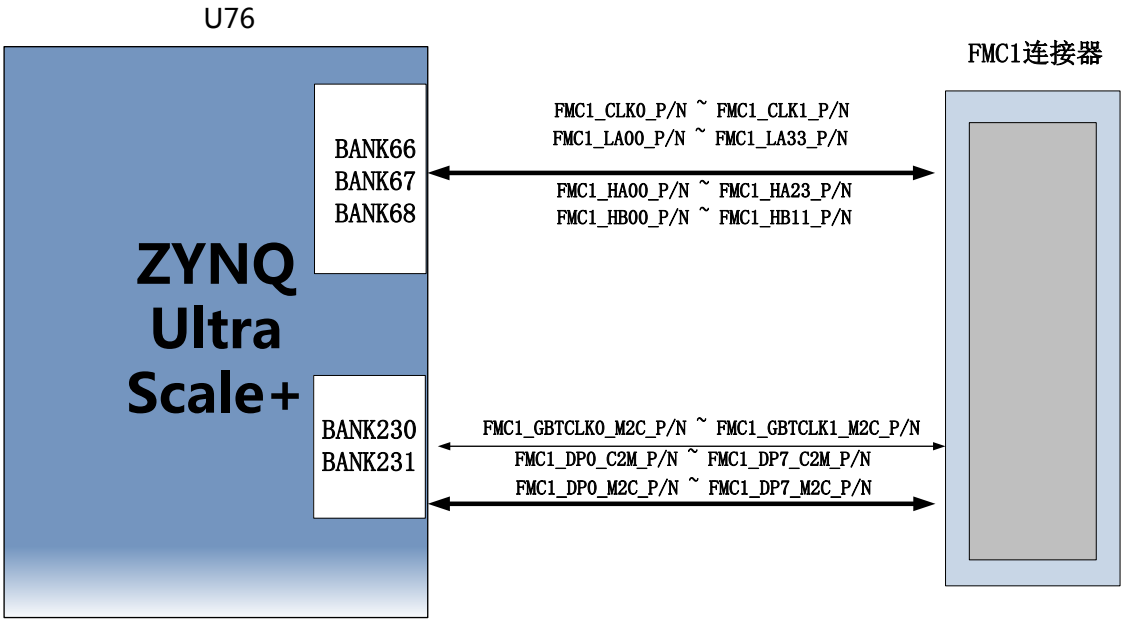


Figure 3-9-1: FMC1 Schematic block

FMC1 connector pin assignment

Signal Name	ZYNQ Pin Name	Pin Number	Description
FMC1_GBTCLK0_M2C_P	230_CLK0_P	V12	FMC Transceiver Reference Clock 0 Positive
FMC1_GBTCLK0_M2C_N	230_CLK0_N	V11	FMC Transceiver Reference Clock 0 Negative
FMC1_GBTCLK1_M2C_P	231_CLK0_P	T12	FMC Transceiver Reference Clock 1 Positive
FMC1_GBTCLK1_M2C_N	231_CLK0_N	T11	FMC Transceiver Reference Clock 1 Negative
FMC1_DP0_M2C_P	230_RX0_P	T4	FMC Transceiver Data RX0 Positive
FMC1_DP0_M2C_N	230_RX0_N	T3	FMC Transceiver Data RX0 Negative
FMC1_DP1_M2C_P	230_RX1_P	R2	FMC Transceiver Data RX1 Positive
FMC1_DP1_M2C_N	230_RX1_N	R1	FMC Transceiver Data RX1 Negative
FMC1_DP2_M2C_P	230_RX2_P	P4	FMC Transceiver Data RX2 Positive
FMC1_DP2_M2C_N	230_RX2_N	P3	FMC Transceiver Data RX2 Negative
FMC1_DP3_M2C_P	230_RX3_P	N2	FMC Transceiver Data RX3 Positive
FMC1_DP3_M2C_N	230_RX3_N	N1	FMC Transceiver Data RX3 Negative
FMC1_DP4_M2C_P	231_RX1_P	L2	FMC Transceiver Data RX4 Positive
FMC1_DP4_M2C_N	231_RX1_N	L1	FMC Transceiver Data RX4 Negative
FMC1_DP5_M2C_P	231_RX3_P	G2	FMC Transceiver Data RX5 Positive
FMC1_DP5_M2C_N	231_RX3_N	G1	FMC Transceiver Data RX5 Negative
FMC1_DP6_M2C_P	231_RX2_P	J2	FMC Transceiver Data RX6 Positive
FMC1_DP6_M2C_N	231_RX2_N	J1	FMC Transceiver Data RX6 Negative

FMC1_DP7_M2C_P	231_RX0_P	M4	FMC Transceiver Data RX7 Positive
FMC1_DP7_M2C_N	231_RX0_N	M3	FMC Transceiver Data RX7 Negative
FMC1_DP0_C2M_P	230_TX0_P	R6	FMC Transceiver Data TX0 Positive
FMC1_DP0_C2M_N	230_TX0_N	R5	FMC Transceiver Data TX0 Negative
FMC1_DP1_C2M_P	230_TX1_P	P8	FMC Transceiver Data TX1 Positive
FMC1_DP1_C2M_N	230_TX1_N	P7	FMC Transceiver Data TX1 Negative
FMC1_DP2_C2M_P	230_TX2_P	N6	FMC Transceiver Data TX2 Positive
FMC1_DP2_C2M_N	230_TX2_N	N5	FMC Transceiver Data TX2 Negative
FMC1_DP3_C2M_P	230_TX3_P	M8	FMC Transceiver Data TX3 Positive
FMC1_DP3_C2M_N	230_TX3_N	M7	FMC Transceiver Data TX3 Negative
FMC1_DP4_C2M_P	231_TX1_P	K4	FMC Transceiver Data TX4 Positive
FMC1_DP4_C2M_N	231_TX1_N	K3	FMC Transceiver Data TX4 Negative
FMC1_DP5_C2M_P	231_TX3_P	H4	FMC Transceiver Data TX5 Positive
FMC1_DP5_C2M_N	231_TX3_N	H3	FMC Transceiver Data TX5 Negative
FMC1_DP6_C2M_P	231_TX2_P	J6	FMC Transceiver Data TX6 Positive
FMC1_DP6_C2M_N	231_TX2_N	J5	FMC Transceiver Data TX6 Negative
FMC1_DP7_C2M_P	231_TX0_P	L6	FMC Transceiver Data TX7 Positive
FMC1_DP7_C2M_N	231_TX0_N	L5	FMC Transceiver Data TX7 Negative
FMC1_CLK0_P	B66_L12_P	AU14	FMC Reference 1st Clock P
FMC1_CLK0_N	B66_L12_N	AV14	FMC Reference 1st Clock N
FMC1_CLK1_P	B67_L12_P	AT11	FMC Reference 2nd Clock P
FMC1_CLK1_N	B67_L12_N	AT10	FMC Reference 2nd Clock N
FMC1_LA00_CC_P	B66_L14_P	AT15	FMC LA 0th Data (Clock) P
FMC1_LA00_CC_N	B66_L14_N	AU15	FMC LA 0th Data (Clock) N
FMC1_LA01_CC_P	B66_L13_P	AV17	FMC LA 1st Data (Clock) P
FMC1_LA01_CC_N	B66_L13_N	AV16	FMC LA 1st Data (Clock) N
FMC1_LA02_P	B66_L3_P	AW17	FMC LA 2nd Data P
FMC1_LA02_N	B66_L3_N	AW16	FMC LA 2nd Data N
FMC1_LA03_P	B66_L1_P	AY17	FMC LA 3rd Data P
FMC1_LA03_N	B66_L1_N	BA17	FMC LA 3rd Data N
FMC1_LA04_P	B66_L4_P	BA15	FMC LA 4th Data P
FMC1_LA04_N	B66_L4_N	BB15	FMC LA 4th Data N
FMC1_LA05_P	B66_L17_P	AR17	FMC LA 5th Data P
FMC1_LA05_N	B66_L17_N	AT17	FMC LA 5th Data N
FMC1_LA06_P	B66_L20_P	AL18	FMC LA 6th Data P
FMC1_LA06_N	B66_L20_N	AM18	FMC LA 6th Data N

FMC1_LA07_P	B66_L22_P	AJ17	FMC LA 7th Data P
FMC1_LA07_N	B66_L22_N	AK17	FMC LA 7th Data N
FMC1_LA08_P	B66_L23_P	AL16	FMC LA 8th Data P
FMC1_LA08_N	B66_L23_N	AM16	FMC LA 8th Data N
FMC1_LA09_P	B66_L21_P	AN18	FMC LA 9th Data P
FMC1_LA09_N	B66_L21_N	AN17	FMC LA 9th Data N
FMC1_LA10_P	B66_L5_P	AY15	FMC LA 10th Data P
FMC1_LA10_N	B66_L5_N	AY14	FMC LA 10th Data N
FMC1_LA11_P	B66_L11_P	AW15	FMC LA 11th Data P
FMC1_LA11_N	B66_L11_N	AW14	FMC LA 11th Data N
FMC1_LA12_P	B66_L19_P	AJ18	FMC LA 12th Data P
FMC1_LA12_N	B66_L19_N	AK18	FMC LA 12th Data N
FMC1_LA13_P	B66_L9_P	BA10	FMC LA 13th Data P
FMC1_LA13_N	B66_L9_N	BB10	FMC LA 13th Data N
FMC1_LA14_P	B66_L7_P	AY12	FMC LA 14th Data P
FMC1_LA14_N	B66_L7_N	BA12	FMC LA 14th Data N
FMC1_LA15_P	B66_L10_P	AU13	FMC LA 15th Data P
FMC1_LA15_N	B66_L10_N	AV13	FMC LA 15th Data N
FMC1_LA16_P	B66_L8_P	BA11	FMC LA 16th Data P
FMC1_LA16_N	B66_L8_N	BB11	FMC LA 16th Data N
FMC1_LA17_CC_P	B67_L14_P	AP10	FMC LA 17th Data (Clock) P
FMC1_LA17_CC_N	B67_L14_N	AR10	FMC LA 17th Data (Clock) N
FMC1_LA18_CC_P	B67_L13_P	AR13	FMC LA 18th Data (Clock) P
FMC1_LA18_CC_N	B67_L13_N	AR12	FMC LA 18th Data (Clock) N
FMC1_LA19_P	B67_L23_P	AM13	FMC LA 19th Data P
FMC1_LA19_N	B67_L23_N	AN13	FMC LA 19th Data N
FMC1_LA20_P	B67_L15_P	AR15	FMC LA 20th Data P
FMC1_LA20_N	B67_L15_N	AR14	FMC LA 20th Data N
FMC1_LA21_P	B67_L11_P	AT13	FMC LA 21st Data P
FMC1_LA21_N	B67_L11_N	AT12	FMC LA 21st Data N
FMC1_LA22_P	B67_L8_P	AU11	FMC LA 22nd Data P
FMC1_LA22_N	B67_L8_N	AV11	FMC LA 22nd Data N
FMC1_LA23_P	B67_L9_P	AW11	FMC LA 23rd Data P
FMC1_LA23_N	B67_L9_N	AW10	FMC LA 23rd Data N
FMC1_LA24_P	B67_L16_P	AN12	FMC LA 24th Data P
FMC1_LA24_N	B67_L16_N	AP12	FMC LA 24th Data N

FMC1_LA25_P	B67_L22_P	AN14	FMC LA 25th Data P
FMC1_LA25_N	B67_L22_N	AP14	FMC LA 25th Data N
FMC1_LA26_P	B67_L7_P	AV12	FMC LA 26th Data P
FMC1_LA26_N	B67_L7_N	AW12	FMC LA 26th Data N
FMC1_LA27_P	B67_L10_P	AV9	FMC LA 27th Data P
FMC1_LA27_N	B67_L10_N	AV8	FMC LA 27th Data N
FMC1_LA28_P	B67_L17_P	AM11	FMC LA 28th Data P
FMC1_LA28_N	B67_L17_N	AN11	FMC LA 28th Data N
FMC1_LA29_P	B67_L1_P	AW9	FMC LA 29th Data P
FMC1_LA29_N	B67_L1_N	AY9	FMC LA 29th Data N
FMC1_LA30_P	B67_L3_P	AW8	FMC LA 30th Data P
FMC1_LA30_N	B67_L3_N	AY8	FMC LA 30th Data N
FMC1_LA31_P	B67_L5_P	BA6	FMC LA 31st Data P
FMC1_LA31_N	B67_L5_N	BB6	FMC LA 31st Data N
FMC1_LA32_P	B67_L2_P	BB9	FMC LA 32nd Data P
FMC1_LA32_N	B67_L2_N	BB8	FMC LA 32nd Data N
FMC1_LA33_P	B67_L4_P	BA8	FMC LA 33rd Data P
FMC1_LA33_N	B67_L4_N	BA7	FMC LA 33rd Data N
FMC1_HA00_CC_P	B68_L11_P	G17	FMC HA 0th Data (Clock) P
FMC1_HA00_CC_N	B68_L11_N	F17	FMC HA 0th Data (Clock) N
FMC1_HA01_CC_P	B68_L12_P	G16	FMC HA 1th Data (Clock) P
FMC1_HA01_CC_N	B68_L12_N	F15	FMC HA 1th Data (Clock) N
FMC1_HA02_P	B68_L2_P	P16	FMC HA 2nd Data P
FMC1_HA02_N	B68_L2_N	N16	FMC HA 2nd Data N
FMC1_HA03_P	B68_L4_P	M15	FMC HA 3rd Data P
FMC1_HA03_N	B68_L4_N	L15	FMC HA 3rd Data N
FMC1_HA04_P	B68_L8_P	J16	FMC HA 4th Data P
FMC1_HA04_N	B68_L8_N	H16	FMC HA 4th Data N
FMC1_HA05_P	B68_L6_P	L17	FMC HA 5th Data P
FMC1_HA05_N	B68_L6_N	K17	FMC HA 5th Data N
FMC1_HA06_P	B68_L9_P	J18	FMC HA 6th Data P
FMC1_HA06_N	B68_L9_N	H18	FMC HA 6th Data N
FMC1_HA07_P	B68_L3_P	M17	FMC HA 7th Data P
FMC1_HA07_N	B68_L3_N	M16	FMC HA 7th Data N
FMC1_HA08_P	B68_L7_P	H15	FMC HA 8th Data P
FMC1_HA08_N	B68_L7_N	G15	FMC HA 8th Data N

FMC1_HA09_P	B68_L5_P	K16	FMC HA 9th Data P
FMC1_HA09_N	B68_L5_N	K15	FMC HA 9th Data N
FMC1_HA10_P	B68_L23_P	D18	FMC LA 10th Data P
FMC1_HA10_N	B68_L23_N	C18	FMC HA 10th Data N
FMC1_HA11_P	B68_L10_P	G18	FMC HA 11th Data P
FMC1_HA11_N	B68_L10_N	F18	FMC HA 11th Data N
FMC1_HA12_P	B68_L21_P	E17	FMC HA 12th Data P
FMC1_HA12_N	B68_L21_N	D17	FMC HA 12th Data N
FMC1_HA13_P	B68_L24_P	B18	FMC HA 13th Data P
FMC1_HA13_N	B68_L24_N	A18	FMC HA 13th Data N
FMC1_HA14_P	B68_L22_P	B17	FMC HA 14th Data P
FMC1_HA14_N	B68_L22_N	A17	FMC HA 14th Data N
FMC1_HA15_P	B68_L20_P	C16	FMC HA 15th Data P
FMC1_HA15_N	B68_L20_N	B16	FMC HA 15th Data N
FMC1_HA16_P	B68_L19_P	E16	FMC HA 16th Data P
FMC1_HA16_N	B68_L19_N	D16	FMC HA 16th Data N
FMC1_HA17_CC_P	B68_L18_P	C15	FMC HA 17th Data (Clock) P
FMC1_HA17_CC_N	B68_L18_N	B15	FMC HA 17th Data (Clock) N
FMC1_HA18_P	B68_L13_P	F14	FMC HA 18th Data P
FMC1_HA18_N	B68_L13_N	E14	FMC HA 18th Data N
FMC1_HA19_P	B68_L1_P	P15	FMC HA 19th Data P
FMC1_HA19_N	B68_L1_N	N15	FMC HA 19th Data N
FMC1_HA20_P	B68_L14_P	E15	FMC HA 20th Data P
FMC1_HA20_N	B68_L14_N	D14	FMC HA 20th Data N
FMC1_HA21_P	B68_L15_P	D13	FMC HA 21th Data P
FMC1_HA21_N	B68_L15_N	C13	FMC HA 21th Data N
FMC1_HA22_P	B68_L17_P	A14	FMC HA 22th Data P
FMC1_HA22_N	B68_L17_N	A13	FMC HA 22th Data N
FMC1_HA23_P	B68_L16_P	B13	FMC HA 23th Data P
FMC1_HA23_N	B68_L16_N	A12	FMC HA 23th Data N
FMC1_HB00_CC_P	B66_L15_P	AU18	FMC HA 0th Data (Clock) P
FMC1_HB00_CC_N	B66_L15_N	AV18	FMC HA 0th Data (Clock) N
FMC1_HB01_P	B66_L16_P	AR18	FMC HB 1th Data P
FMC1_HB01_N	B66_L16_N	AT18	FMC HB 1th Data N
FMC1_HB02_P	B66_L24_P	AN16	FMC HB 2nd Data P
FMC1_HB02_N	B66_L24_N	AP16	FMC HB 2nd Data N

FMC1_HB03_P	B66_L18_P	AT16	FMC HB 3rd Data P
FMC1_HB03_N	B66_L18_N	AU16	FMC HB 3rd Data N
FMC1_HB04_P	B66_L2_P	BA16	FMC HB 4th Data P
FMC1_HB04_N	B66_L2_N	BB16	FMC HB 4th Data N
FMC1_HB05_P	B66_L6_P	BA13	FMC HB 5th Data P
FMC1_HB05_N	B66_L6_N	BB13	FMC HB 5th Data N
FMC1_HB06_CC_P	B67_L21_P	AL14	FMC HB 6th Data P
FMC1_HB06_CC_N	B67_L21_N	AM14	FMC HB 6th Data N
FMC1_HB07_P	B67_L24_P	AJ14	FMC HB 7th Data P
FMC1_HB07_N	B67_L24_N	AK14	FMC HB 7th Data N
FMC1_HB08_P	B67_L19_P	AL15	FMC HA 8th Data P
FMC1_HB08_N	B67_L19_N	AM15	FMC HB 8th Data N
FMC1_HB09_P	B67_L20_P	AJ15	FMC HB 9th Data P
FMC1_HB09_N	B67_L20_N	AK15	FMC HB 9th Data N
FMC1_HB10_P	B67_L18_P	AM10	FMC HB 10th Data P
FMC1_HB10_N	B67_L18_N	AN10	FMC HB 0th Data N
FMC1_HB11_P	B67_L6_P	BB5	FMC HA 11th Data P
FMC1_HB11_N	B67_L6_N	BB4	FMC HB 11th Data N
FMC1_SCL	B94_L5_N	D3	FMC I2C clock
FMC1_SDA	B94_L5_P	D4	FMC I2C data

The design diagram of ZYNQ Ultrascale+ and FMC1 connectors is shown in Figure 3-9-2.

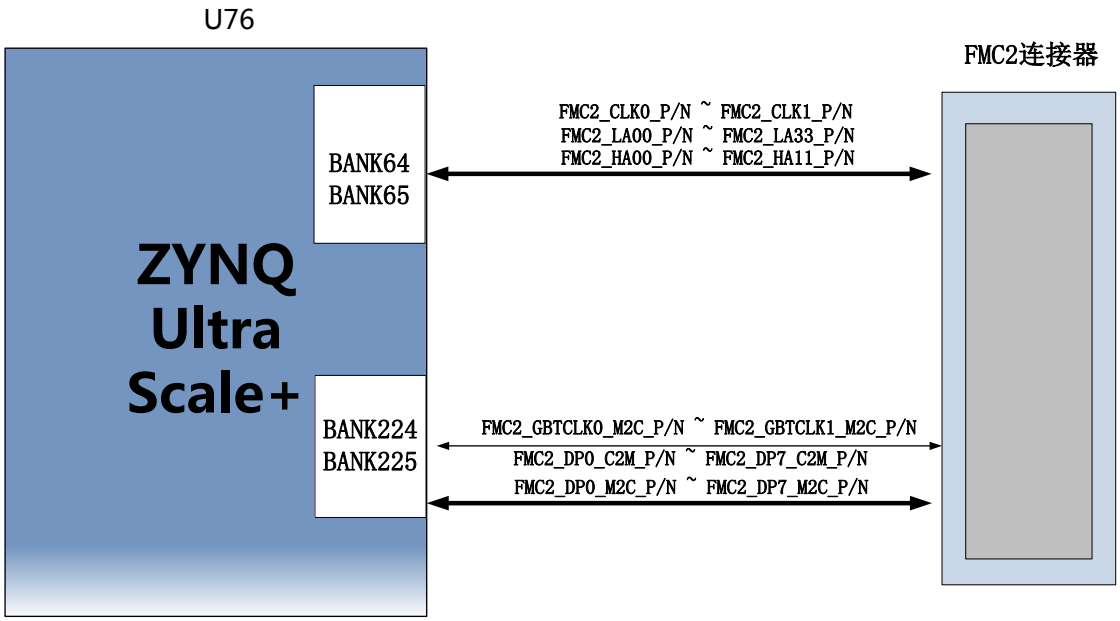


Figure 3-9-2: FMC1 Schematic block

FMC2 connector pin assignment

Signal Name	ZYNQ Pin Name	Pin Number	Description
FMC2_GBTCLK0_M2C_P	131_CLK1_P	J32	FMC Transceiver Reference Clock 0 Positive
FMC2_GBTCLK0_M2C_N	131_CLK1_N	J33	FMC Transceiver Reference Clock 0 Negative
FMC2_GBTCLK1_M2C_P	130_CLK1_P	N32	FMC Transceiver Reference Clock 1 Positive
FMC2_GBTCLK1_M2C_N	130_CLK1_N	N33	FMC Transceiver Reference Clock 1 Negative
FMC2_DP0_C2M_P	131_TX3_P	E36	FMC Transceiver Data RX0 Positive
FMC2_DP0_C2M_N	131_TX3_N	E37	FMC Transceiver Data RX0 Negative
FMC2_DP3_C2M_P	131_TX2_P	F34	FMC Transceiver Data RX1 Positive
FMC2_DP3_C2M_N	131_TX2_N	F35	FMC Transceiver Data RX1 Negative
FMC2_DP1_C2M_P	131_TX1_P	G36	FMC Transceiver Data RX2 Positive
FMC2_DP1_C2M_N	131_TX1_N	G37	FMC Transceiver Data RX2 Negative
FMC2_DP2_C2M_P	131_TX0_P	H34	FMC Transceiver Data RX3 Positive
FMC2_DP2_C2M_N	131_TX0_N	H35	FMC Transceiver Data RX3 Negative
FMC2_DP4_C2M_P	130_TX2_P	K34	FMC Transceiver Data RX4 Positive
FMC2_DP4_C2M_N	130_TX2_N	K35	FMC Transceiver Data RX4 Negative
FMC2_DP5_C2M_P	130_TX0_P	M34	FMC Transceiver Data RX5 Positive
FMC2_DP5_C2M_N	130_TX0_N	M35	FMC Transceiver Data RX5 Negative
FMC2_DP6_C2M_P	130_TX1_P	L36	FMC Transceiver Data RX6 Positive
FMC2_DP6_C2M_N	130_TX1_N	L37	FMC Transceiver Data RX6 Negative

FMC2_DP7_C2M_P	130_TX3_P	J36	FMC Transceiver Data RX7 Positive
FMC2_DP7_C2M_N	130_TX3_N	J37	FMC Transceiver Data RX7 Negative
FMC2_DP0_M2C_P	131_RX3_P	D39	FMC Transceiver Data TX0 Positive
FMC2_DP0_M2C_N	131_RX3_N	D40	FMC Transceiver Data TX0 Negative
FMC2_DP1_M2C_P	131_RX1_P	F39	FMC Transceiver Data TX1 Positive
FMC2_DP1_M2C_N	131_RX1_N	F40	FMC Transceiver Data TX1 Negative
FMC2_DP2_M2C_P	131_RX0_P	G41	FMC Transceiver Data TX2 Positive
FMC2_DP2_M2C_N	131_RX0_N	G42	FMC Transceiver Data TX2 Negative
FMC2_DP3_M2C_P	131_RX2_P	E41	FMC Transceiver Data TX3 Positive
FMC2_DP3_M2C_N	131_RX2_N	E42	FMC Transceiver Data TX3 Negative
FMC2_DP4_M2C_P	130_RX2_P	J41	FMC Transceiver Data TX4 Positive
FMC2_DP4_M2C_N	130_RX2_N	J42	FMC Transceiver Data TX4 Negative
FMC2_DP5_M2C_P	130_RX0_P	L41	FMC Transceiver Data TX5 Positive
FMC2_DP5_M2C_N	130_RX0_N	L42	FMC Transceiver Data TX5 Negative
FMC2_DP6_M2C_P	130_RX1_P	K39	FMC Transceiver Data TX6 Positive
FMC2_DP6_M2C_N	130_RX1_N	K40	FMC Transceiver Data TX6 Negative
FMC2_DP7_M2C_P	130_RX3_P	H39	FMC Transceiver Data TX7 Positive
FMC2_DP7_M2C_N	130_RX3_N	H40	FMC Transceiver Data TX7 Negative
FMC2_CLK0_N	B65_L11_N	AU26	FMC Reference 1st Clock P
FMC2_CLK0_P	B65_L11_P	AU25	FMC Reference 1st Clock N
FMC2_CLK1_P	B64_L12_P	AU20	FMC Reference 2nd Clock P
FMC2_CLK1_N	B64_L12_N	AV19	FMC Reference 2nd Clock N
FMC2_LA00_CC_N	B65_L13_N	AT27	FMC LA 0th Data (Clock) P
FMC2_LA00_CC_P	B65_L13_P	AR27	FMC LA 0th Data (Clock) N
FMC2_LA01_CC_N	B65_L12_N	AT26	FMC LA 1st Data (Clock) P
FMC2_LA01_CC_P	B65_L12_P	AT25	FMC LA 1st Data (Clock) N
FMC2_LA02_N	B65_L18_N	AT28	FMC LA 2nd Data P
FMC2_LA02_P	B65_L18_P	AR28	FMC LA 2nd Data N
FMC2_LA03_N	B65_L15_N	AN26	FMC LA 3rd Data P
FMC2_LA03_P	B65_L15_P	AM26	FMC LA 3rd Data N
FMC2_LA04_N	B65_L10_N	AV28	FMC LA 4th Data P
FMC2_LA04_P	B65_L10_P	AU28	FMC LA 4th Data N
FMC2_LA05_N	B65_L16_N	AP27	FMC LA 5th Data P
FMC2_LA05_P	B65_L16_P	AN27	FMC LA 5th Data N
FMC2_LA06_N	B65_L5_N	AY28	FMC LA 6th Data P
FMC2_LA06_P	B65_L5_P	AY27	FMC LA 6th Data N

FMC2_LA07_N	B65_L4_N	BB26	FMC LA 7th Data P
FMC2_LA07_P	B65_L4_P	BA26	FMC LA 7th Data N
FMC2_LA08_N	B65_L3_N	BA25	FMC LA 8th Data P
FMC2_LA08_P	B65_L3_P	AY25	FMC LA 8th Data N
FMC2_LA09_N	B65_L2_N	BB25	FMC LA 9th Data P
FMC2_LA09_P	B65_L2_P	BB24	FMC LA 9th Data N
FMC2_LA10_N	B65_L24_N	AK24	FMC LA 10th Data P
FMC2_LA10_P	B65_L24_P	AJ24	FMC LA 10th Data N
FMC2_LA11_N	B65_L20_N	AP25	FMC LA 11th Data P
FMC2_LA11_P	B65_L20_P	AP24	FMC LA 11th Data N
FMC2_LA12_N	B65_L1_N	AY24	FMC LA 12th Data P
FMC2_LA12_P	B65_L1_P	AW24	FMC LA 12th Data N
FMC2_LA13_N	B65_L22_N	AN23	FMC LA 13th Data P
FMC2_LA13_P	B65_L22_P	AM23	FMC LA 13th Data N
FMC2_LA14_N	B65_L19_N	AT23	FMC LA 14th Data P
FMC2_LA14_P	B65_L19_P	AR23	FMC LA 14th Data N
FMC2_LA15_N	B65_L23_N	AL23	FMC LA 15th Data P
FMC2_LA15_P	B65_L23_P	AK23	FMC LA 15th Data N
FMC2_LA16_N	B65_L21_N	AN24	FMC LA 16th Data P
FMC2_LA16_P	B65_L21_P	AM24	FMC LA 16th Data N
FMC2_LA17_CC_P	B64_L14_P	AT20	FMC LA 17th Data (Clock) P
FMC2_LA17_CC_N	B64_L14_N	AU19	FMC LA 17th Data (Clock) N
FMC2_LA18_CC_P	B64_L13_P	AT22	FMC LA 18th Data (Clock) P
FMC2_LA18_CC_N	B64_L13_N	AT21	FMC LA 18th Data (Clock) N
FMC2_LA19_P	B64_L24_P	AJ22	FMC LA 19th Data P
FMC2_LA19_N	B64_L24_N	AK22	FMC LA 19th Data N
FMC2_LA20_P	B64_L16_P	AN21	FMC LA 20th Data P
FMC2_LA20_N	B64_L16_N	AP21	FMC LA 20th Data N
FMC2_LA21_P	B64_L22_P	AK20	FMC LA 21st Data P
FMC2_LA21_N	B64_L22_N	AK19	FMC LA 21st Data N
FMC2_LA22_P	B64_L23_P	AJ21	FMC LA 22nd Data P
FMC2_LA22_N	B64_L23_N	AJ20	FMC LA 22nd Data N
FMC2_LA23_P	B64_L20_P	AM21	FMC LA 23rd Data P
FMC2_LA23_N	B64_L20_N	AM20	FMC LA 23rd Data N
FMC2_LA24_P	B64_L15_P	AN22	FMC LA 24th Data P
FMC2_LA24_N	B64_L15_N	AP22	FMC LA 24th Data N

FMC2_LA25_P	B64_L3_P	BA22	FMC LA 25th Data P
FMC2_LA25_N	B64_L3_N	BA21	FMC LA 25th Data N
FMC2_LA26_P	B64_L19_P	AM19	FMC LA 26th Data P
FMC2_LA26_N	B64_L19_N	AN19	FMC LA 26th Data N
FMC2_LA27_P	B64_L21_P	AL22	FMC LA 27th Data P
FMC2_LA27_N	B64_L21_N	AL21	FMC LA 27th Data N
FMC2_LA28_P	B64_L17_P	AP20	FMC LA 28th Data P
FMC2_LA28_N	B64_L17_N	AR20	FMC LA 28th Data N
FMC2_LA29_P	B64_L7_P	AU23	FMC LA 29th Data P
FMC2_LA29_N	B64_L7_N	AV23	FMC LA 29th Data N
FMC2_LA30_P	B64_L11_P	AU21	FMC LA 30th Data P
FMC2_LA30_N	B64_L11_N	AV21	FMC LA 30th Data N
FMC2_LA31_P	B64_L9_P	AW20	FMC LA 31st Data P
FMC2_LA31_N	B64_L9_N	AW19	FMC LA 31st Data N
FMC2_LA32_P	B64_L8_P	AV22	FMC LA 32nd Data P
FMC2_LA32_N	B64_L8_N	AW22	FMC LA 32nd Data N
FMC2_LA33_P	B64_L10_P	AY19	FMC LA 33rd Data P
FMC2_LA33_N	B64_L10_N	AY18	FMC LA 33rd Data N
FMC2_HA00_CC_N	B65_L9_N	AW27	FMC HA 0th Data (Clock) P
FMC2_HA00_CC_P	B65_L9_P	AV27	FMC HA 0th Data (Clock) N
FMC2_HA01_CC_N	B65_L17_N	AN28	FMC HA 1th Data (Clock) P
FMC2_HA01_CC_P	B65_L17_P	AM28	FMC HA 1th Data (Clock) N
FMC2_HA02_N	B65_L8_N	AW26	FMC HA 2nd Data P
FMC2_HA02_P	B65_L8_P	AV26	FMC HA 2nd Data N
FMC2_HA03_N	B65_L6_N	BB28	FMC HA 3rd Data P
FMC2_HA03_P	B65_L6_P	BA28	FMC HA 3rd Data N
FMC2_HA04_N	B65_L14_N	AR25	FMC HA 4th Data P
FMC2_HA04_P	B65_L14_P	AR24	FMC HA 4th Data N
FMC2_HA05_N	B65_L7_N	AV24	FMC HA 5th Data P
FMC2_HA05_P	B65_L7_P	AU24	FMC HA 5th Data N
FMC2_HA06_P	B64_L1_P	BA23	FMC HA 6th Data P
FMC2_HA06_N	B64_L1_N	BB23	FMC HA 6th Data N
FMC2_HA07_N	B64_L2_P	AY23	FMC HA 7th Data P
FMC2_HA07_P	B64_L2_N	AY22	FMC HA 7th Data N
FMC2_HA08_P	B64_L5_P	BB20	FMC HA 8th Data P
FMC2_HA08_N	B64_L5_N	BB19	FMC HA 8th Data N

FMC2_HA09_P	B64_L6_P	BA18	FMC HA 9th Data P
FMC2_HA09_N	B64_L6_N	BB18	FMC HA 9th Data N
FMC2_HA10_P	B64_L4_P	AY20	FMC LA 10th Data P
FMC2_HA10_N	B64_L4_N	BA20	FMC HA 10th Data N
FMC2_HA11_P	B64_L18_P	AP19	FMC HA 11th Data P
FMC2_HA11_N	B64_L18_N	AR19	FMC HA 11th Data N
FMC2_SCL	B90_L1_N	N10	FMC I2C clock
FMC2_SDA	B90_L1_P	N11	FMC I2C data

Part 3.10: JTAG Debug Port

The JTAG interface is reserved on Z19-P for downloading or debugging ZYNQ UltraScale+ programs or firmware.

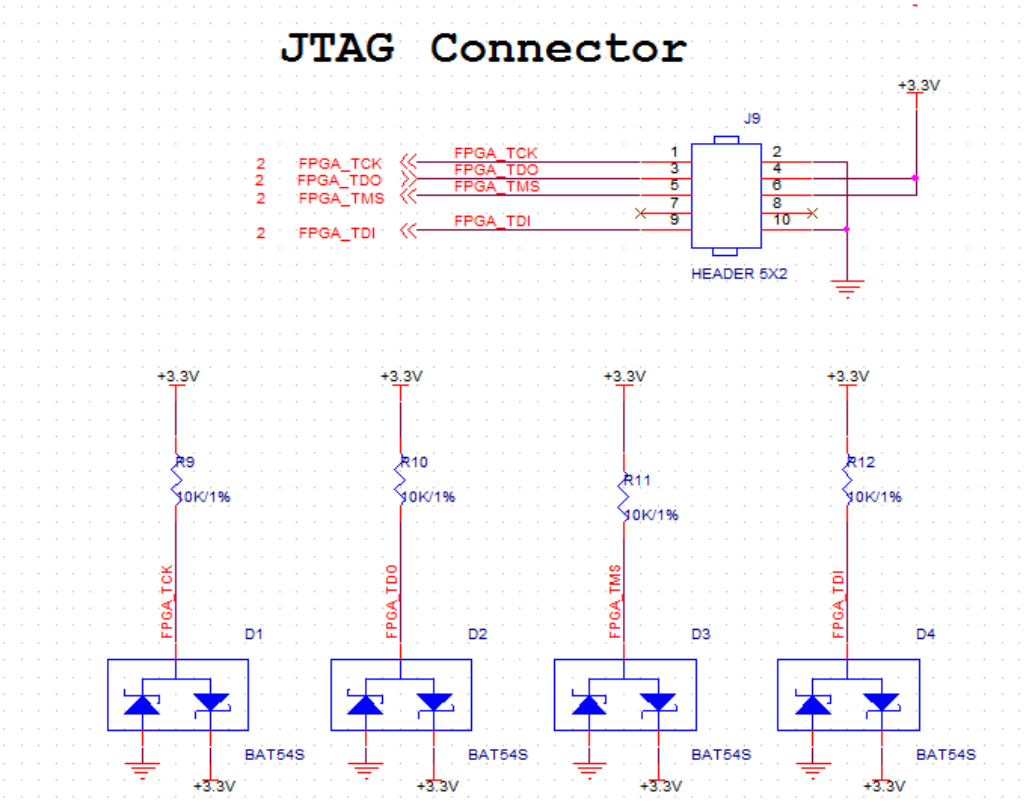


Figure 3-10-1: JTAG Interface Schematic

Part 3.11: EEPROM and Temperature Sensor

The Z19-P development board has an EEPROM onboard. The P/N of the EEPROM is 24LC04, and the capacity is: 4Kbit (2 * 256 * 8bit), which is

connected to the PS terminal through the I2C bus.

A high-precision, low-power, digital temperature sensor chip is installed on the Z19-P development board, and the P/N is LM75. The temperature accuracy of the LM75 chip is 0.5 degrees.

Figure 3-11-1 is the schematic diagram of EEPROM and temperature sensor

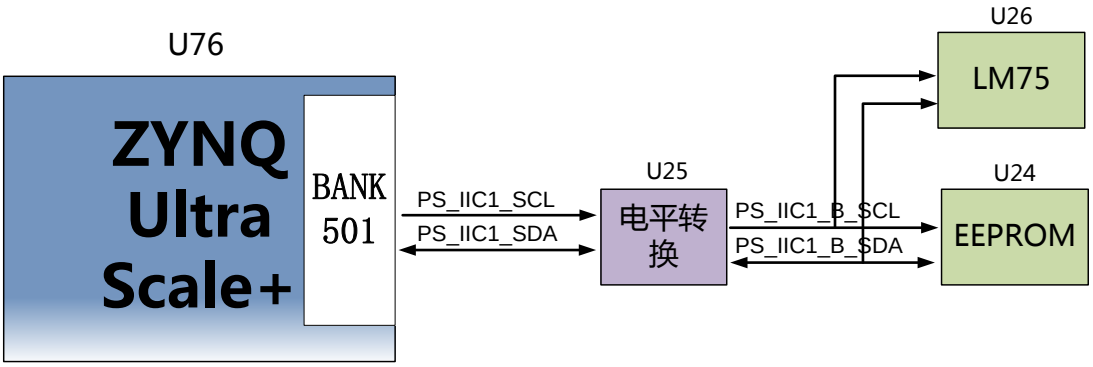


Figure 3-11-1: EEPROM and Sensor connection diagram

EEPROM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_IIC1_SDA	PS_MIO25_500	AG34	I2C Clock Signal
PS_IIC1_SCL	PS_MIO24_500	AH33	I2C Data Signal

Part 3.12: User LEDs

There are 4 LEDs on the Z19-P Carrier board. including 1 power LED, 1 DONE LED, 1 PS control LED, and 1 PL control LED. The schematic diagram of the LED hardware connection is shown in Figure 3-12-1:

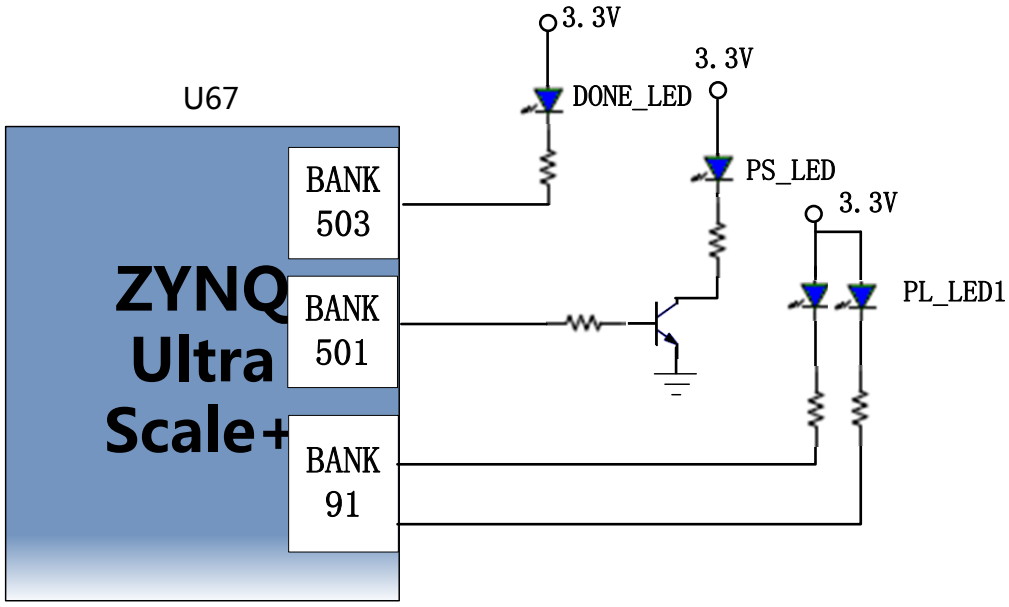


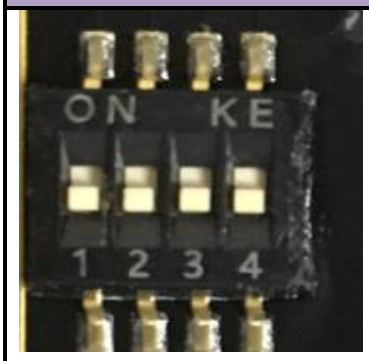
Figure 3-12-1: The LEDs Hardware Connection Diagram

Pin assignment of user LED lights

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_LED	PS_MIO31	M28	PS User LED Light
TEST_LED1	B91_L7_N	E10	PL User LED1 Light
TEST_LED2	B91_L7_P	E11	PL User LED2 Light

Part 3.13: MODE Switch Configuration

There is a 4-digit switch SW1 on the Z19-P carrier board to configure the boot mode of the ZYNQ system. The ZYNQ system supports 4 boot modes. The 4 boot modes are JTAG debug mode, QSPI FLASH, EMMC and SD2.0 card mode. When ZU19EG chipset is powered on, it will detect the voltage level of (PS_MODE0~3) to determine the boot mode. The user can select different boot modes through the SW1. The SW1 boot mode configuration is shown in the following table 3-13-1.

SW1	Dial Position（1，2，3，4）	MODE[3:0]	Start mode
	ON，ON，ON，ON	0000	PS JTAG
	ON，ON，OFF ,ON	0010	QSPI FLASH
	ON，OFF，ON，OFF	0101	SD Card
	ON，OFF， OFF， ON	0110	EMMC

3-13-1 boot mode configuration

Part 3.14 Power Supply

The power input voltage of the Z19-P carrier board is DC12V. the DC12V is converted into +5V, +3.3V, +1.8V, FMC1_VADJ and FMC2_VADJ. The design diagram of the power supply design on the board is shown in Figure 3-14-1:

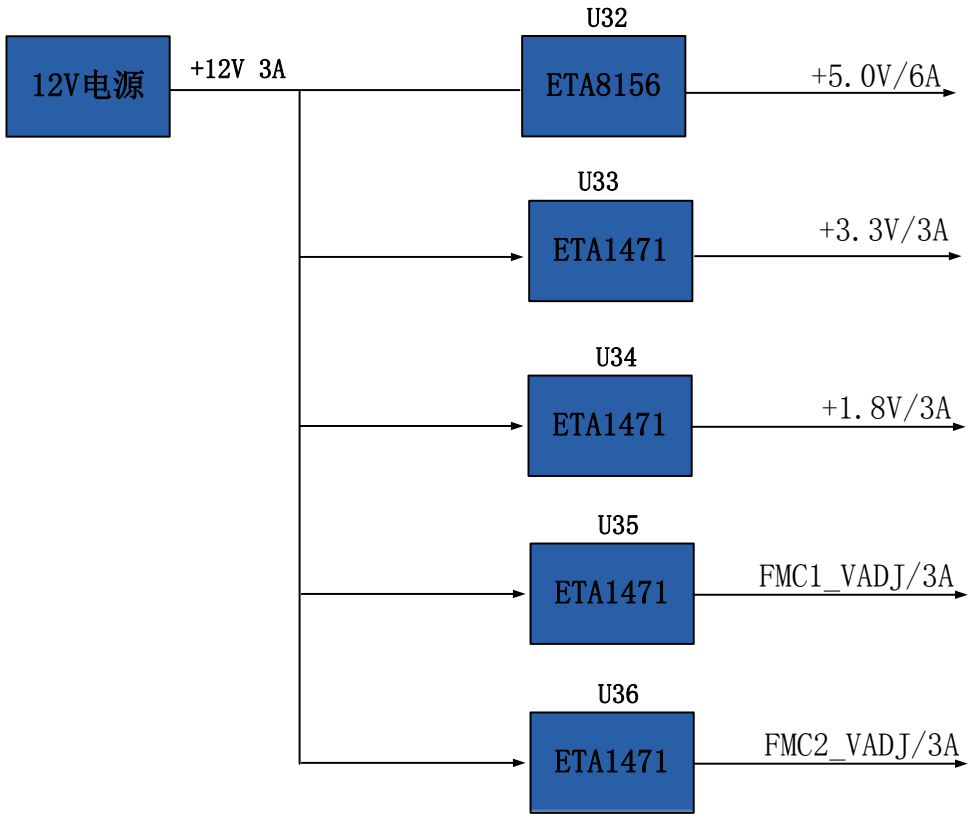


Figure 3-14-1: Carrier Board Power Design

The functions of each power distribution are shown in the following table:

Power	Function
+5.0V	USB power supply
+1.8V	Ethernet, USB2.0
+3.3V	Ethernet, USB2.0, SD, DP
FMC1_VADJ	FMC1
FMC2_VADJ	FMC2

Part 3.15: Fan

Because ZU19EG generates a lot of heat when it works normally, we add a heat sink and fan to prevent the chip from overheating. The fan is controlled by the BANK50 IO (PIN J10) of ZYNQ. If the IO output is low, the MOSFET is turned on and the fan is working. If the IO level output is high, the fan stops. The fan design on the board is shown in Figure 3-15-1.

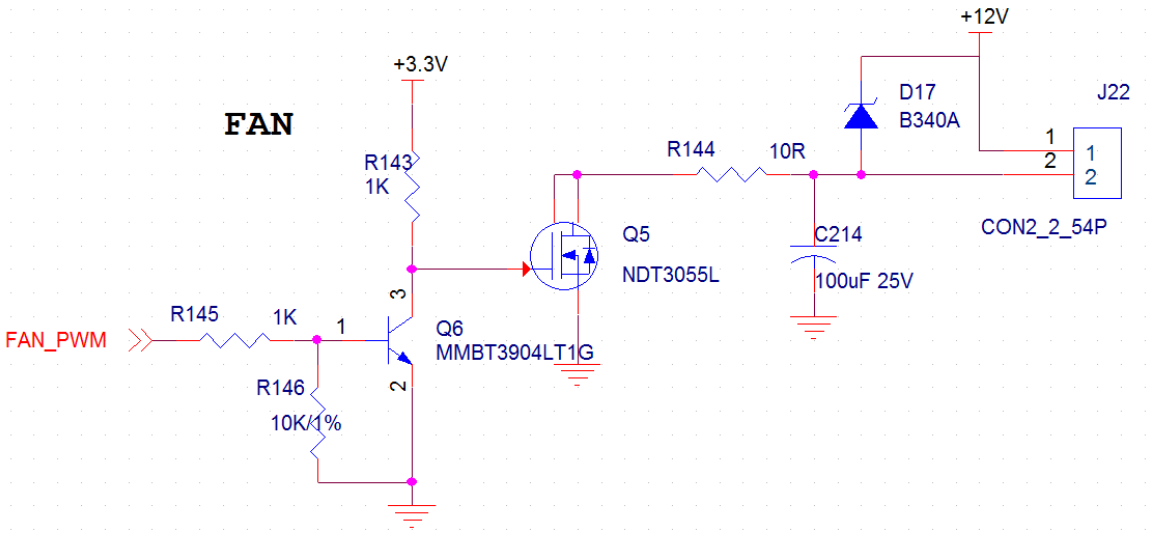


Figure 3-15-1：Fan Design Schematic

Part 3.16: Carrier Board Mechanical

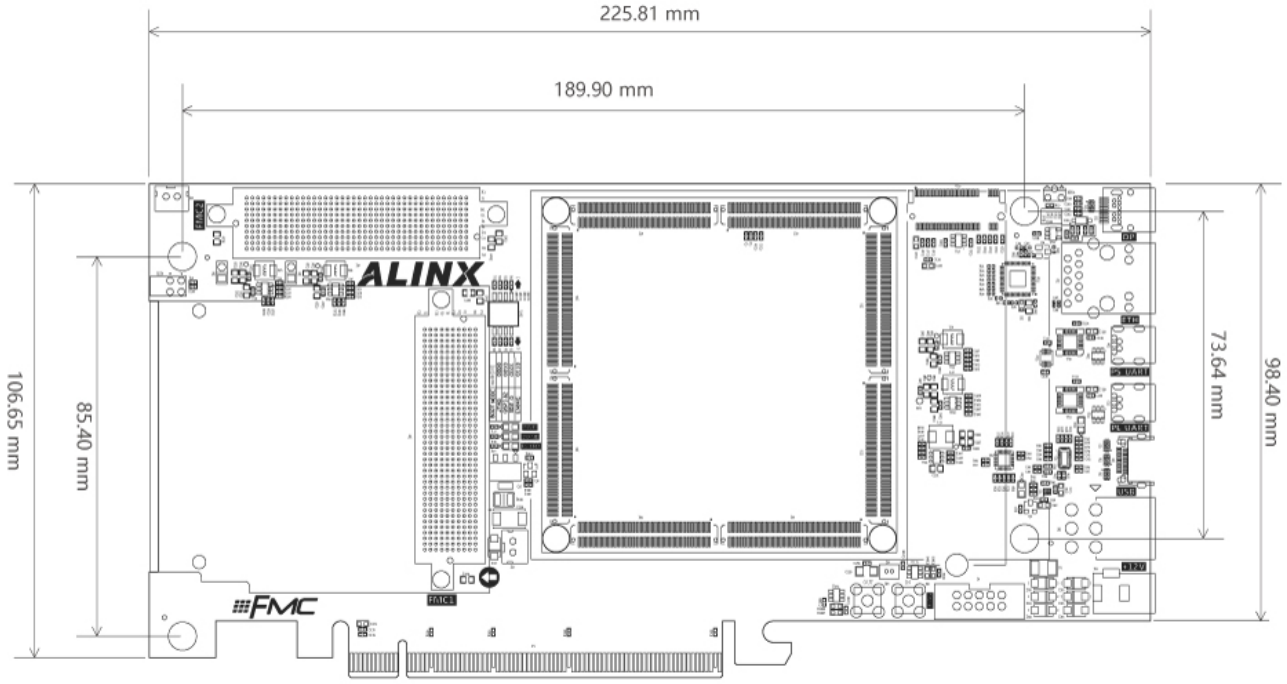


Figure 3-16-1: Carrier Board Mechanical