FMC Binocular MIPI Camera Module FL0214

User Manual

ALINX

Table of Contents

Part1: FL0214 Binocular MIPI Camera Module General Description

ALINX FMC Binocular MIPI Module FL0214 is a 2-channel 1.3 megapixel CMOS camera module with MIPI interface. The FL0214 module has two MIPI interface camera modules. The camera module uses Sony's CMOS sensor chip IMX21. The camera has a maximum resolution of 4224 (horizontal) x 3120 (vertical). The camera's MIPI signal is converted to an LVDS signal by the MC20901 chip to the FMC interface for FPGA sampling.

The module has a standard LPC FMC interface for connecting to the FPGA development board. The FMC connector model is: ASP_134604_01

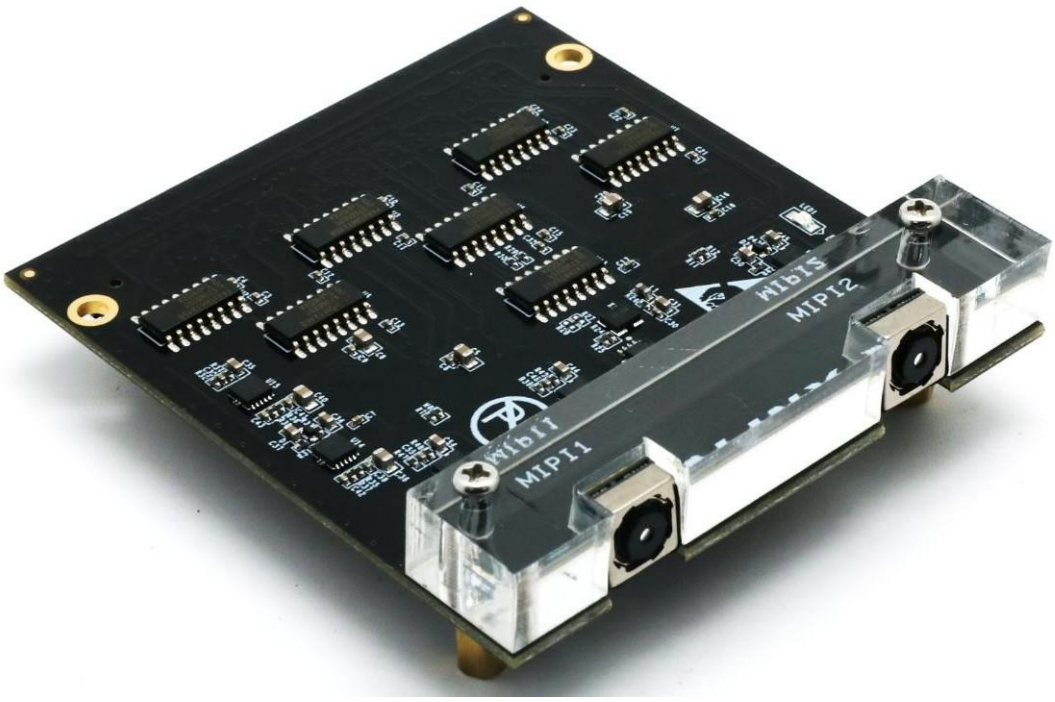

Figure 1-1: FL0214 module product photo

Part 1.1: FL0214 Module Detail Parameter

FL0214 Binocular MIPI Camera module detail parameter listed as below:

- CMOS image sensor chip: SONY IMX214
- Full resolution @30fps (Normal / HDR). 4K2K @30fps (Normal / HDR) 1080p @60fps (Normal / HDR)
- Output video format of RAW10/8, COMP8/6.
- Focusing distance: 10CM ~ infinity
- Focusing mode: Motor auto focus
- Viewing angle: 80.7° ± 3° (Diag)
- CSI-2 serial data output (MIPI 4lane, D-PHY spec. ver. 1.1 compliant)
- Camera configuration interface: I2C
- MC20901 driver chip: level shifting (MIPI D-PHY->LVDS):
- Working temperature: -20 ˚C ~ 65 ˚C

Part 1.2: FL0214 Module Size Dimension

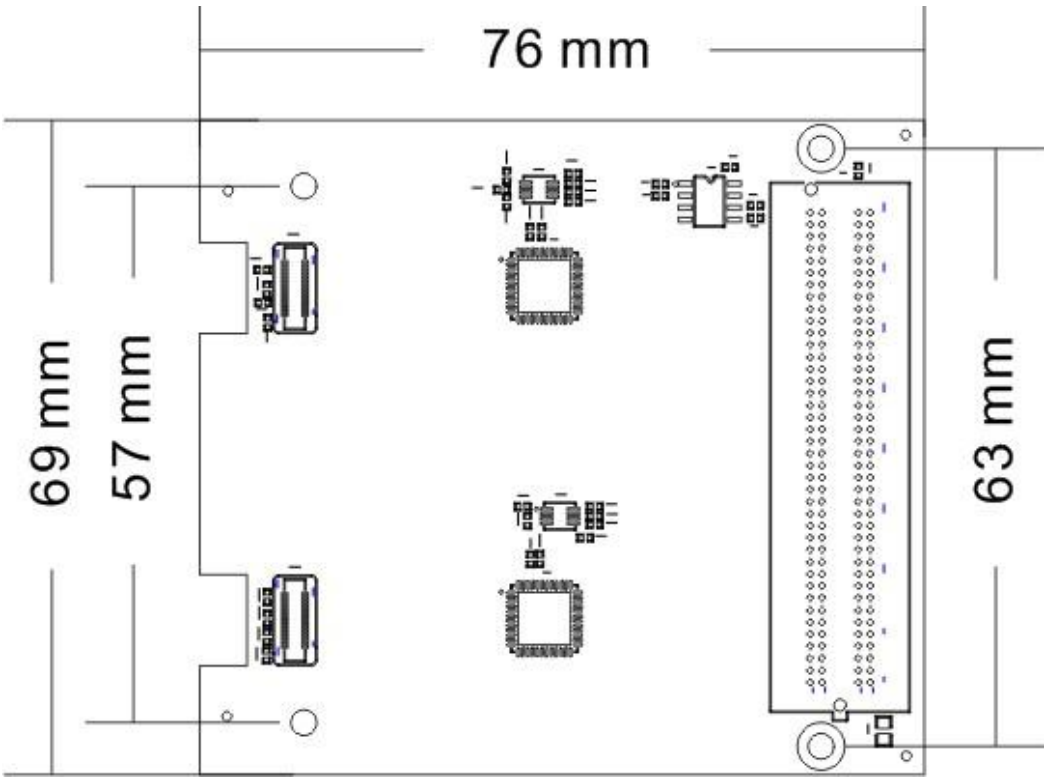

Figure 1-2: FL0214 Binocular MIPI Camera Module Dimensions

Part 2: FL0214 Module Function Description

Part 2.1: FL0214 Module Block Diagram

Figure 2-1: FL0214 Module Block Diagram as below:

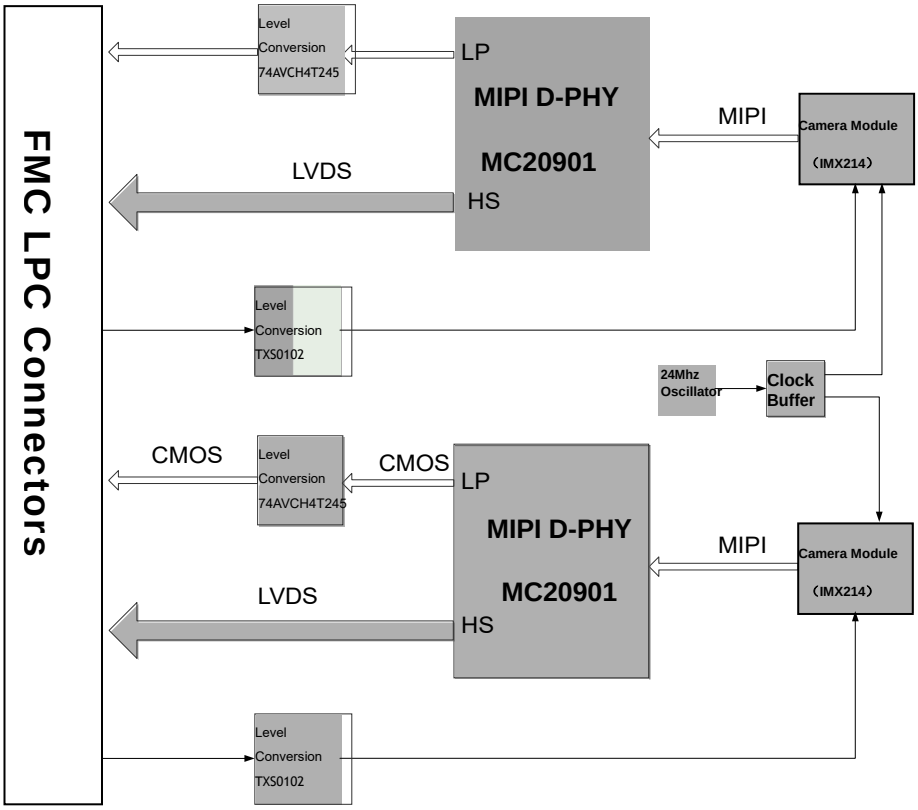

Figure 2-1: FL0214 Module Block Diagram

Part 2.2: FL0214 Binocular MIPI Camera Module

FL0214 Binocular MIPI Camera Module, make the lens motor drive and CMOS sensor chip on a module. The panel size of the module is 8.5mm*8.5mm and the viewing angle is 80.7°. CMOS uses SONY's IMX214 sensor with a resolution of 130,000 pixels. The module can control the internal registers and control the motor through the I2C bus to achieve focus adjustment. The I2C write device address is 0x20 and the read device address is 0x21. Refer to the documentation for the IMX214 for specific information on the registers. Refer to

the documentation of the IMX214 for specific register information.

Part 2.3: MC20901 5 Channel FPGA Bridge IC for MIPI D-PHY Systems and SLVS to LVDS Conversion

Since the interface of the FPGA does not directly support the level standard of the MIPI D-PHY, a bridge chip MC20901 is required for level conversion. The MC20901 is a 5-channel MIPI D-PHY circuit conversion chip. The 4-channel LANE data output by the camera and the MIPI signal of the 1-channel clock LANE are converted into LVDS differential signals supported by the FPGA chip through the MC20901 chip. The following Figure 2-2 shows the functional block diagram of the first CHA channel of the MC20901:

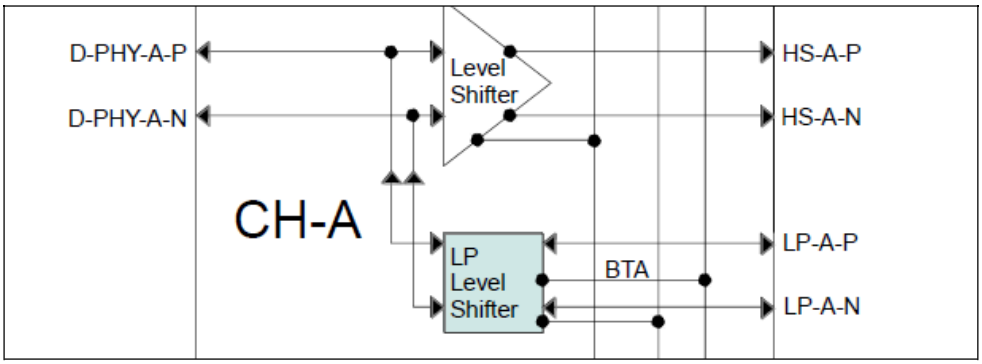

Figure 2-2：Functional block diagram of the first CHA channel of the MC20901

Part 2.4: FL0214 Module FMC LPC pin assignment

Only the signals of the power supply and interface are listed below. The signal of GND is not listed. For details, please refer to the schematic

Pin Number	Signal Name	Description
C35	+12V	12V Power Input
C37	+12V	12V Power Input
D32	+3.3V	3.3V Power Input
C34	GA0	Bit0 of EEPROM address
D35	GA1	Bit1 of EEPROM address
D9	CSI1_CMOS_LP_CLK_N	The 1st channel camera CMOS clock negative output

D8	CSI1_CMOS_LP_CLK_P	The 1st channel camera CMOS clock positive output
G16	CSI1_CMOS_LP0_N	The 1st channel camera CMOS LANE0 data negative output
G15	CSI1_CMOS_LP0_P	The 1st channel camera CMOS LANE0 data positive output
G13	CSI1_CMOS_LP1_N	The 1st channel camera CMOS LANE1 data negative output
G12	CSI1_CMOS_LP1_P	The 1st channel camera CMOS LANE1 data positive output
G19	CSI1_CMOS_LP2_N	The 1st channel camera CMOS LANE2 data negative output
G18	CSI1_CMOS_LP2_P	The 1st channel camera CMOS LANE2 data positive output
G10	CSI1_CMOS_LP3_N	The 1st channel camera CMOS LANE3 data negative output
G9	CSI1_CMOS_LP3_P	The 1st channel camera CMOS LANE3 data positive output
G7	CSI1_LVDS_CLK_N	The 1st channel camera LVDS clock negative output
G6	CSI1_LVDS_CLK_P	The 1st channel camera LVDS clock positive output
H14	CSI1_LVDS_HS0_N	The 1st channel camera LVDS LANE0 data negative output
H13	CSI1_LVDS_HS0_P	The 1st channel camera LVDS LANE0 data positive output
H11	CSI1_LVDS_HS1_N	The 1st channel camera LVDS LANE1 negative output
H10	CSI1_LVDS_HS1_P	The 1st channel camera LVDS LANE1 data positive output
H17	CSI1_LVDS_HS2_N	The 1st channel camera LVDS LANE2 data negative output
H16	CSI1_LVDS_HS2_P	The 1st channel camera LVDS LANE2 data positive output
H8	CSI1_LVDS_HS3_N	The 1st channel camera LVDS LANE3 data negative output
H7	CSI1_LVDS_HS3_P	The 1st channel camera LVDS LANE3 data positive output
G21	CSI1_OTP_B	The 1st channel camera programming interface
D26	CSI1_RST_N	The 1st channel camera Reset signal input
D21	CSI2_CMOS_LP_CLK_N	The 2nd channel camera CMOS clock negative output
D20	CSI2_CMOS_LP_CLK_P	The 2nd channel camera CMOS clock

		positive output
G34	CSI2_CMOS_LP0_N	The 2nd channel camera CMOS LANE0 data negative output
G33	CSI2_CMOS_LP0_P	The 2nd channel camera CMOS LANE0 data positive output
G28	CSI2_CMOS_LP1_N	The 2nd channel camera CMOS LANE1 data negative output
G27	CSI2_CMOS_LP1_P	The 2nd channel camera CMOS LANE1 data positive output
G37	CSI2_CMOS_LP2_N	The 2nd channel camera CMOS LANE2 data negative output
G36	CSI2_CMOS_LP2_P	The 2nd channel camera CMOS LANE2 data positive output
G25	CSI2_CMOS_LP3_N	The 2nd channel camera CMOS LANE3 data negative output
G24	CSI2_CMOS_LP3_P	The 2nd channel camera CMOS LANE3 data positive output
C23	CSI2_LVDS_CLK_N	The 2nd channel camera LVDS clock negative output
C22	CSI2_LVDS_CLK_P	The 2nd channel camera LVDS clock positive output
H29	CSI2_LVDS_HS0_N	The 2nd channel camera LVDS LANE0 data negative output
H28	CSI2_LVDS_HS0_P	The 2nd channel camera LVDS LANE0 data positive output
H26	CSI2_LVDS_HS1_N	The 2nd channel camera LVDS LANE1 negative output
H25	CSI2_LVDS_HS1_P	The 2nd channel camera LVDS LANE1 data positive output
H32	CSI2_LVDS_HS2_N	The 2nd channel camera LVDS LANE2 data negative output
H31	CSI2_LVDS_HS2_P	The 2nd channel camera LVDS LANE2 data positive output
H23	CSI2_LVDS_HS3_N	The 2nd channel camera LVDS LANE3 data negative output
H22	CSI2_LVDS_HS3_P	The 2nd channel camera LVDS LANE3 data positive output
C27	CSI2_OTP_B	The 2nd channel camera programming interface
D27	CSI2_RST_N	The 2nd channel camera Reset signal input
D14	FMC_CSI1_SCL	The 1st channel camera IIC bus clock
D15	FMC_CSI1_SDA	The 1st channel camera IIC bus data
H37	FMC_CSI2_SCL	The 2nd channel camera IIC bus clock
H38	FMC_CSI2_SDA	The 2nd channel camera IIC bus data

C34	GA0	EEPROM I2C address 0
D35	GA1	EEPROM I2C address 0
C30	SCL	EEPROM I2C clock
C31	SDA	EEPROM I2C data
G39	VADJ	VADJ Power Input
H40	VADJ	VADJ Power Input

Part 3: Hardware Connection and Testing

The hardware connection between the FL0214 module and the FPGA development board is very simple. Simply plug the FL0214 FMC interface into the FMC interface of the FPGA development board and fix it with screws. The following is the hardware connection diagram of the ALINX AX7350 development board and FL0214:

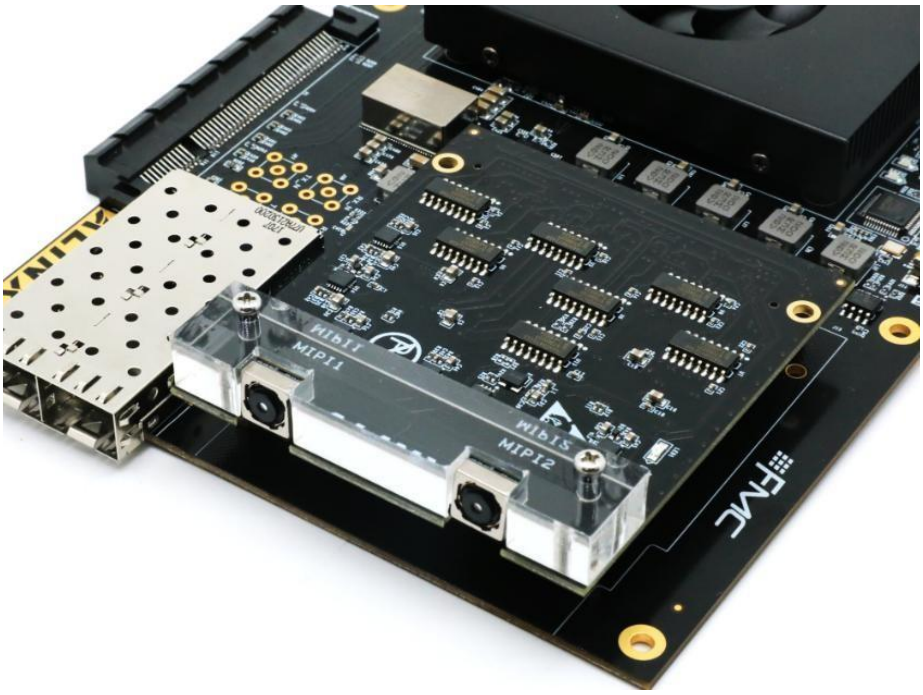

Figure 3-1: Hardware Connection

In the VIVADO software development environment, download the binocular test routine to the FPGA development board, through the HDMI output interface of the FPGA development board, and the video image of FL0214 Binocular MIPI Camera Module to the HDMI monitor. The single video display effect is as follow Figure 3-2:

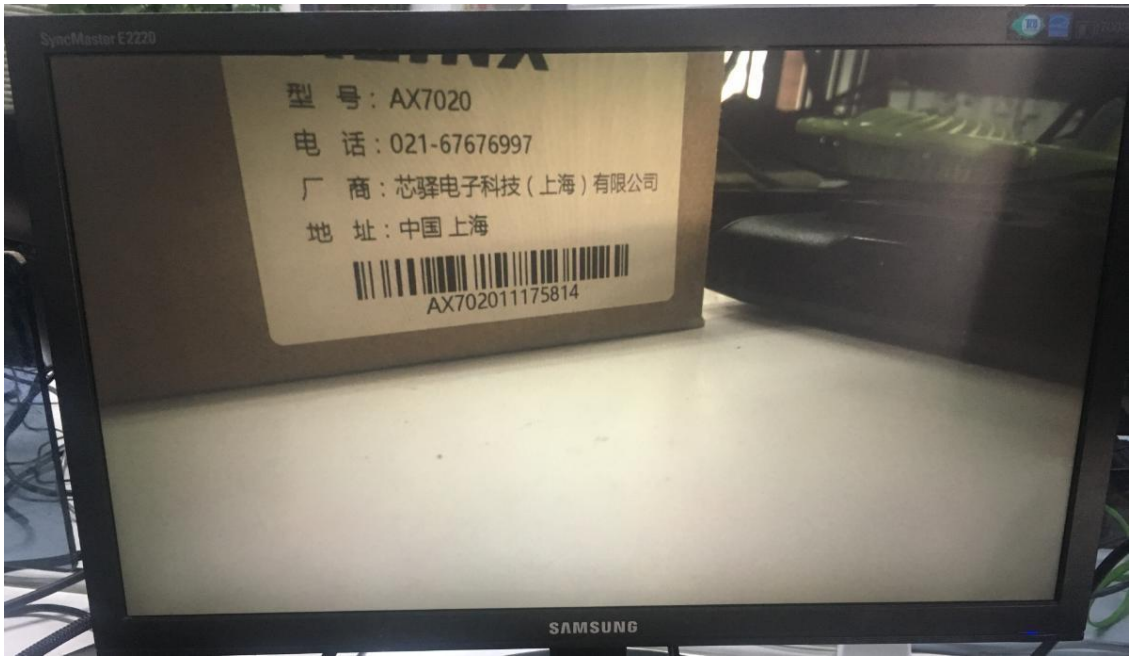

Figure 3-2: The single video display effect