ZYNQ7000 FPGA Development Board AX7350B

User Manual

ALINX

Version Record

Revision	Date	Release By	Description
Rev 1.0	2019-04-05	Rachel Zhou	First Release

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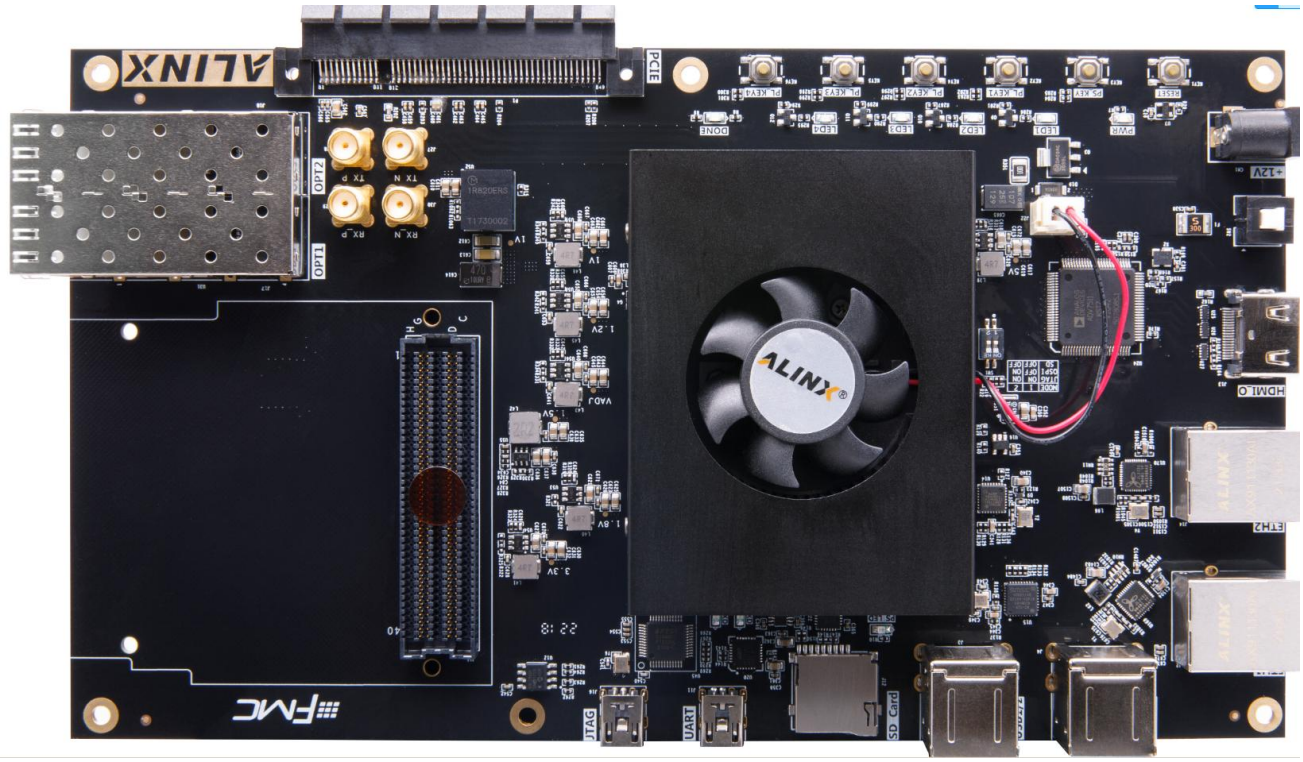
The ZYNQ7000 FPGA development platform uses XILINX's Zynq7000 SOC chip XC7Z035 solution, which uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. ZYNQ has two 512MB high-speed DDR3 SDRAM chips on the PS and PL sides. In addition, there are one 8GB eMMC memory chip and one 256Mb QSPI FLASH chip on the PS side.

In terms of peripheral circuits, we have extended a wealth of interfaces for users, such as a PCIex4 slot, 2 fiber interfaces, 2 Gigabit Ethernet interfaces, 4 USB2.0 HOST interfaces, 1 HDMI output interface, 1 channel UART serial interface, 1 SD card interface, and an FMC expansion interface. It meets users' requirements for high-speed data exchange, data storage, video transmission processing and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in ZYNQ development.



Part 1: FPGA Development Board Introduction

The AX7350B FPGA development board is mainly composed of ZYNQ7350 main chip, 4 DDR3, 1 eMMC, 1 QSPI FLASH and some peripheral interfaces. The ZYNQ7350 uses Xilinx's Zynq7000 series of chips, model number XC7Z035-2FFG676. The ZYNQ7035 chip can be divided into Processor System (PS) and Programmable Logic (PL). On the PS and PL sides of the ZYNQ7350 chip, two DDR3s are mounted, each with a DDR3 capacity of up to 512 Mbytes. The ARM system and the FPGA system can independently process and store data. The PS-side 8GB eMMC FLASH memory chip and 256Mb QSPI FLASH are used to statically store ZYNQ's operating system, file system and user data.

The AX7350B FPGA development board expands its rich peripheral interface, including one PCIex4 slot, two SFP interfaces, two Gigabit Ethernet interfaces, four USB2.0 HOST interfaces, one HDMI output interface, and one UART serial interface. 1 SD card interface, 1 FMC expansion interface and some button LEDs.

Figure 1-1 is the Schematic diagram of the entire FPGA development boards:

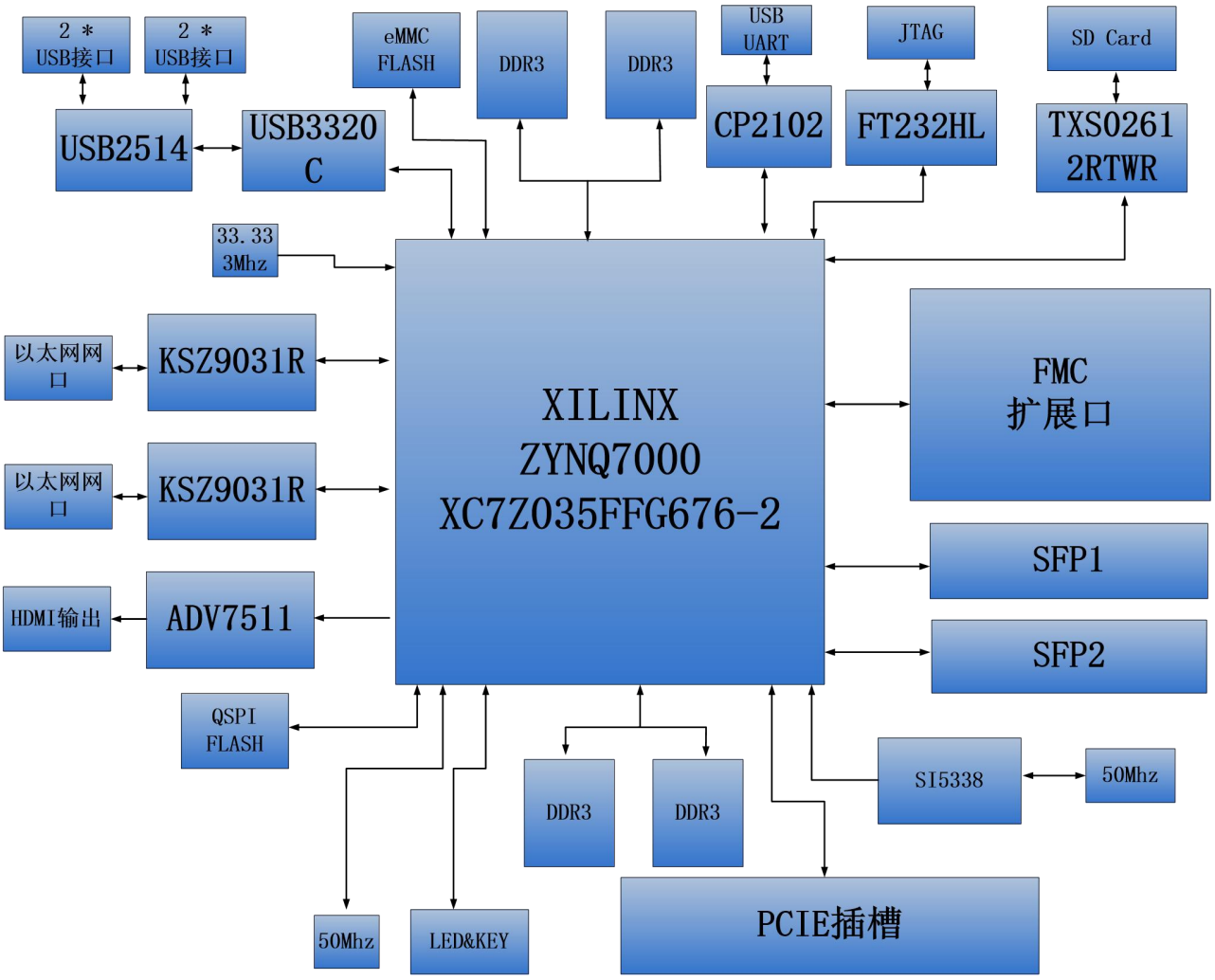


Figure 1-1: The Schematic Diagram of the AX7350B

Through this diagram, you can see the interfaces and functions that the AX7350B FPGA Development Board contains:

- Xilinx ARM+FPGA chip Zynq-7000 XC7Z035-2FFG676
- DDR3

  With four large-capacity 512M bytes (2GB total), high-speed DDR3 SDRAM. Two of them are mounted on the PS side, which can be used as a buffer for ZYNQ chip data, or as a memory for the operating system. The other two are attached to the PL end and can be used as data storage, image analysis cache, and data processing of the FPGA.
- eMMC

The PS side mounts an 8GB eMMC FLASH memory chip to store user operating system files or other user data.

- QSPI FLASH

  A 256Mbit QSPI FLASH memory chip can be used as a Uboot file for ZYNQ chips, storage of system files and user data;

- PCIe x4 Interface

  The standard PCIEx8 host slot is used for PCIEx4 communication, and can be used to connect PCIEx4, x2, x1 PCIE boards for PCIE data communication. Support the PCI Express 2.0 standard with single channel communication, rates up to 5GBaud.

- 2 SFP Interface

  The 2-channel high-speed transceiver of ZYNQ's GTX transceiver is connected to the transmission and reception of two optical modules to realize two high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds of up to 10 Gb/s.

- Gigabite Ethernet Interface

  2-channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses JLSemi JL2121-N040I industrial grade GPHY chip, one Ethernet is connected to the PS end of the ZYNQ chip, and one Ethernet is connected to the PL end of the ZYNQ chip.

- HDMI video output

  1 channel HDMI video output interface, selected ADV7511 HDMI encoding chip of ANALOG DEVICE, up to 1080P@60Hz output, support 3D output.

- USB2.0 HOST Interface

  Extend the 4-channe USB HOST interface through the USB Hub chip for connecting external USB slave devices, such as connecting a

mouse, keyboard, USB flash drive etc. The USB interface uses a flat USB interface (USB Type A).

- USB Uart Interface

  2-way Uart to USB interfaces for communication with the computer, for user debugging. 1 channel on the core board, Used for the core board works independently; 1 way is on the bottom board, and used for the whole board debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- Micro SD card holder

  1-channel Micro SD card holder, for save operating system images and file systems.

- FMC expansion port

  A standard FMC LPC expansion port for connecting XILINX or ALINXDE various FMC modules (HDMI input and output modules, binocular camera modules, high-speed AD modules etc.). The FMC expansion port contains 34 pairs of differential IO signals and one high-speed GTX transceiver signal.

- USB JTAG Interface

  One way USB JTAG port, debug and download ZYNQ system through USB cable and onboard JTAG circuit

- Clock

  An on-board 33.333Mhz active crystal oscillator provides a stable clock source for the PS system, a 50MHz active crystal oscillator that provides additional clocking for the PL logic, and a programmable clock chip on the board that provides the clock source for the GTX. Provide a reference clock for PCIE, SFP and DDR operation.

- LED Light

  9 LEDs, 1 power indicator; 1 DONE configuration indicator; 2 serial

communication indicators, 1 PS control LED, 4 PL control indicators.

- Button

  6 buttons, 1 reset button, 1 PS user button, 4 PL user buttons

Part 2: ZYNQ Chip

The AX7350B FPGA development board uses Xilinx's Zynq7000 series chip, model XC7Z035-2FFG676. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power up or reset. Figure 2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

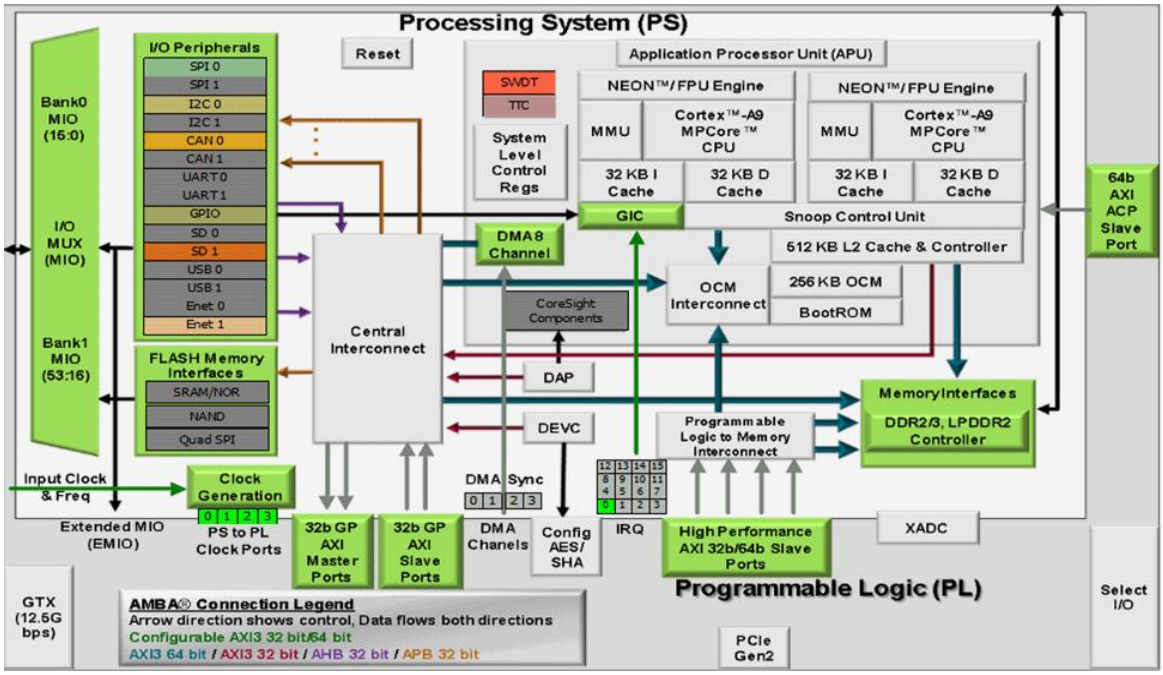


Figure 2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 54 multi-function IOs that can be configured as normal IO or peripheral control interfaces
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 275K
- Look-up-tables (LUTs): 171,900
- Flip-flops: 343,800
- 18x25MACCs：900
- Block RAM：17.6Mb
- 8-channel high-speed GTX transceiver, supporting PCIE Gen2x8;
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z020-2CLG484I chip speed grade is -2, industrial grade, package is

FGG676, pin pitch is 1.0mm the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2

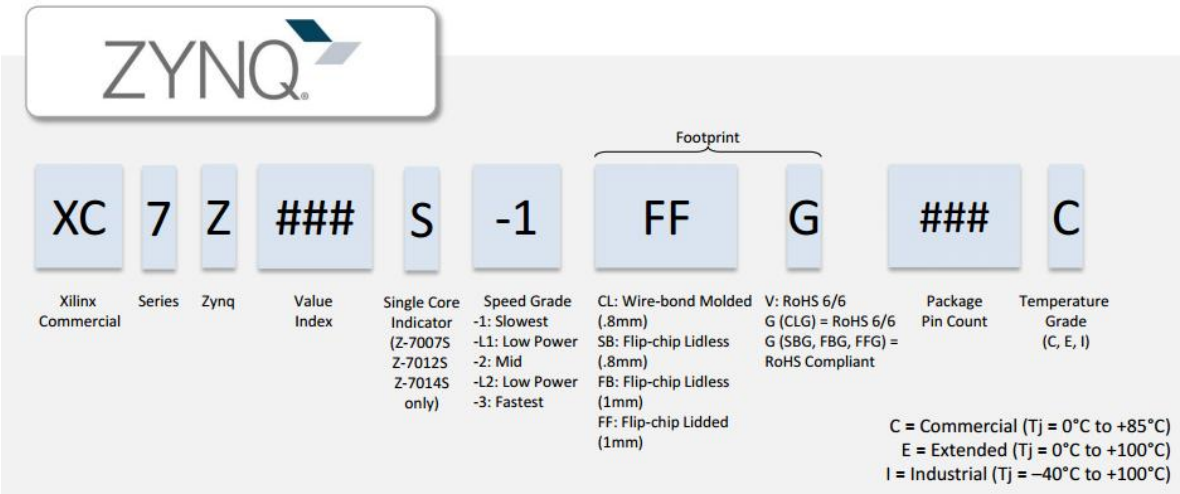


Figure 2-2: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-3: The XC7Z035 chip used on the Core Board

Part 3: DDR3 DRAM

The AX7350B FPGA development board is equipped with four Micron 512MB DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125), in which Two DDR3s are mounted on the PS and PL sides. Two DDR3 SDRAMs form a 32-bit bus width. The PS-side DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps), and two DDR3 memory systems are directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The PL-side DDR3 SDRAM has a maximum operating speed of 800MHz (data rate 1600Mbps), and two DDR3 memory systems are connected to the BANK33 and BANK34 interfaces of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 3-1.

Bit Number	Chip Model	Capacity	Factory
U4,U5,U7,U8	MT41J256M16HA-125	256M x 16bit	Micron

Table 3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

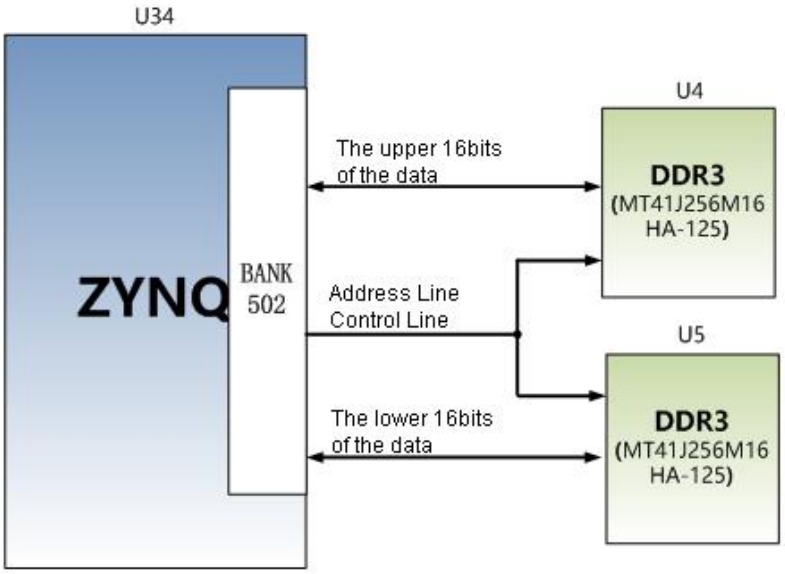


Figure 3-1: The Schematic Part of DDR3 DRAM on the PS side

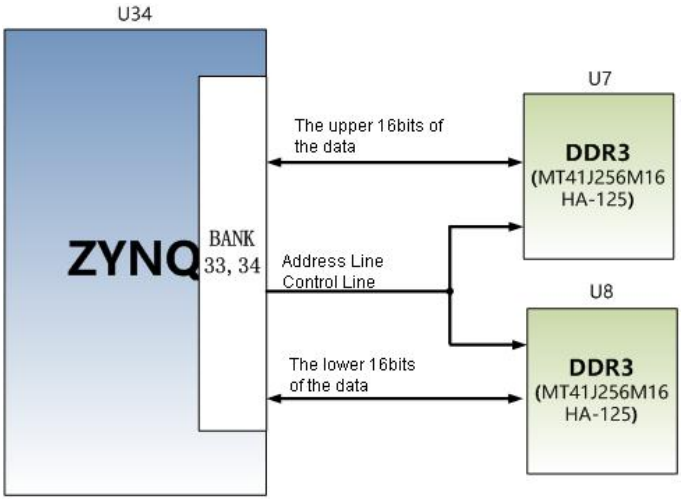


Figure 3-2: The Schematic Part of DDR3 DRAM on the PL side

PS side DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	H24
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	G25
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	L24
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	L25
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	P25
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	R25

PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	W24
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	W25
PS_DDR3_D0	PS_DDR_DQ0_502	J26
PS_DDR3_D1	PS_DDR_DQ1_502	F25
PS_DDR3_D2	PS_DDR_DQ2_502	J25
PS_DDR3_D3	PS_DDR_DQ3_502	G26
PS_DDR3_D4	PS_DDR_DQ4_502	H26
PS_DDR3_D5	PS_DDR_DQ5_502	H23
PS_DDR3_D6	PS_DDR_DQ6_502	J24
PS_DDR3_D7	PS_DDR_DQ7_502	J23
PS_DDR3_D8	PS_DDR_DQ8_502	K26
PS_DDR3_D9	PS_DDR_DQ9_502	L23
PS_DDR3_D10	PS_DDR_DQ10_502	M26
PS_DDR3_D11	PS_DDR_DQ11_502	K23
PS_DDR3_D12	PS_DDR_DQ12_502	M25
PS_DDR3_D13	PS_DDR_DQ13_502	N24
PS_DDR3_D14	PS_DDR_DQ14_502	M24
PS_DDR3_D15	PS_DDR_DQ15_502	N23
PS_DDR3_D16	PS_DDR_DQ16_502	R26
PS_DDR3_D17	PS_DDR_DQ17_502	P24
PS_DDR3_D18	PS_DDR_DQ18_502	N26
PS_DDR3_D19	PS_DDR_DQ19_502	P23
PS_DDR3_D20	PS_DDR_DQ20_502	T24
PS_DDR3_D21	PS_DDR_DQ21_502	T25
PS_DDR3_D22	PS_DDR_DQ22_502	T23
PS_DDR3_D23	PS_DDR_DQ23_502	R23
PS_DDR3_D24	PS_DDR_DQ24_502	V24
PS_DDR3_D25	PS_DDR_DQ25_502	U26
PS_DDR3_D26	PS_DDR_DQ26_502	U24
PS_DDR3_D27	PS_DDR_DQ27_502	U25
PS_DDR3_D28	PS_DDR_DQ28_502	W26
PS_DDR3_D29	PS_DDR_DQ29_502	Y25
PS_DDR3_D30	PS_DDR_DQ30_502	Y26
PS_DDR3_D31	PS_DDR_DQ31_502	W23
PS_DDR3_DM0	PS_DDR_DM0_502	G24
PS_DDR3_DM1	PS_DDR_DM1_502	K25

PS_DDR3_DM2	PS_DDR_DM2_502	P26
PS_DDR3_DM3	PS_DDR_DM3_502	V26
PS_DDR3_A0	PS_DDR_A0_502	K22
PS_DDR3_A1	PS_DDR_A1_502	K20
PS_DDR3_A2	PS_DDR_A2_502	N21
PS_DDR3_A3	PS_DDR_A3_502	L22
PS_DDR3_A4	PS_DDR_A4_502	M20
PS_DDR3_A5	PS_DDR_A5_502	N22
PS_DDR3_A6	PS_DDR_A6_502	L20
PS_DDR3_A7	PS_DDR_A7_502	J21
PS_DDR3_A8	PS_DDR_A8_502	T20
PS_DDR3_A9	PS_DDR_A9_502	U20
PS_DDR3_A10	PS_DDR_A10_502	M22
PS_DDR3_A11	PS_DDR_A11_502	H21
PS_DDR3_A12	PS_DDR_A12_502	P20
PS_DDR3_A13	PS_DDR_A13_502	J20
PS_DDR3_A14	PS_DDR_A14_502	R20
PS_DDR3_BA0	PS_DDR_BA0_502	U22
PS_DDR3_BA1	PS_DDR_BA1_502	T22
PS_DDR3_BA2	PS_DDR_BA2_502	R22
PS_DDR3_S0	PS_DDR_CS_B_502	Y21
PS_DDR3_RAS	PS_DDR_RAS_B_502	V23
PS_DDR3_CAS	PS_DDR_CAS_B_502	Y23
PS_DDR3_WE	PS_DDR_WE_B_502	V22
PS_DDR3_ODT	PS_DDR_ODT_502	Y22
PS_DDR3_RESET	PS_DDR_DRST_B_502	H22
PS_DDR3_CLK0_P	PS_DDR_CKP_502	R21
PS_DDR3_CLK0_N	PS_DDR_CKN_502	P21
PS_DDR3_CKE	PS_DDR_CKE_502	U21

PL side DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_33	G2
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_33	F2
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_33	K2

PL_DDR3_DQS1_N	IO_L9N_T1_DQS_33	K1
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_33	N3
PL_DDR3_DQS2_N	IO_L15N_T2_DQS_33	N2
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_33	M8
PL_DDR3_DQS4_N	IO_L21N_T3_DQS_33	L8
PL_DDR3_D0	IO_L5N_T0_33	E1
PL_DDR3_D1	IO_L1N_T0_33	F4
PL_DDR3_D2	IO_L4P_T0_33	D1
PL_DDR3_D3	IO_L1P_T0_33	G4
PL_DDR3_D4	IO_L2N_T0_33	D3
PL_DDR3_D5	IO_L5P_T0_33	E2
PL_DDR3_D6	IO_L2P_T0_33	D4
PL_DDR3_D7	IO_L4N_T0_33	C1
PL_DDR3_D8	IO_L7N_T1_33	H1
PL_DDR3_D9	IO_L10N_T1_33	G1
PL_DDR3_D10	IO_L7P_T1_33	J1
PL_DDR3_D11	IO_L8N_T1_33	H3
PL_DDR3_D12	IO_L11N_T1_SRCC_33	K3
PL_DDR3_D13	IO_L8P_T1_33	H4
PL_DDR3_D14	IO_L11P_T1_SRCC_33	L3
PL_DDR3_D15	IO_L10P_T1_33	H2
PL_DDR3_D16	IO_L18P_T2_33	N1
PL_DDR3_D17	IO_L14P_T2_SRCC_33	L5
PL_DDR3_D18	IO_L14N_T2_SRCC_33	L4
PL_DDR3_D19	IO_L13P_T2_MRCC_33	M6
PL_DDR3_D20	IO_L16P_T2_33	M2
PL_DDR3_D21	IO_L17P_T2_33	N4
PL_DDR3_D22	IO_L16N_T2_33	L2
PL_DDR3_D23	IO_L17N_T2_33	M4
PL_DDR3_D24	IO_L23P_T3_33	N7
PL_DDR3_D25	IO_L22N_T3_33	J6
PL_DDR3_D26	IO_L19P_T3_33	M7
PL_DDR3_D27	IO_L20N_T3_33	J5
PL_DDR3_D28	IO_L24P_T3_33	K8
PL_DDR3_D29	IO_L20P_T3_33	K5
PL_DDR3_D30	IO_L24N_T3_33	K7

PL_DDR3_D31	IO_L22P_T3_33	K6
PL_DDR3_DM0	IO_L6P_T0_33	F3
PL_DDR3_DM1	IO_L12P_T1_MRCC_33	J4
PL_DDR3_DM2	IO_L13N_T2_MRCC_33	M5
PL_DDR3_DM3	IO_L23N_T3_33	N6
PL_DDR3_A0	IO_L17N_T2_34	A8
PL_DDR3_A1	IO_L23P_T3_34	C2
PL_DDR3_A2	IO_L14P_T2_SRCC_34	D6
PL_DDR3_A3	IO_L15N_T2_DQS_34	B9
PL_DDR3_A4	IO_L10N_T1_34	D5
PL_DDR3_A5	IO_L17P_T2_34	A9
PL_DDR3_A6	IO_L11N_T1_SRCC_34	E7
PL_DDR3_A7	IO_L15P_T2_DQS_34	C9
PL_DDR3_A8	IO_L12N_T1_MRCC_34	F7
PL_DDR3_A9	IO_L18N_T2_34	A7
PL_DDR3_A10	IO_L24N_T3_34	A2
PL_DDR3_A11	IO_L11P_T1_SRCC_34	F8
PL_DDR3_A12	IO_L23N_T3_34	B1
PL_DDR3_A13	IO_L16P_T2_34	B10
PL_DDR3_A14	IO_L12P_T1_MRCC_34	G7
PL_DDR3_BA0	IO_L18P_T2_34	B7
PL_DDR3_BA1	IO_L19N_T3_VREF_34	C3
PL_DDR3_BA2	IO_L22N_T3_34	A3
PL_DDR3_S0	IO_L14N_T2_SRCC_34	C6
PL_DDR3_RAS	IO_L19P_T3_34	C4
PL_DDR3_CAS	IO_L20N_T3_34	B4
PL_DDR3_WE	IO_L20P_T3_34	B5
PL_DDR3_ODT	IO_L22P_T3_34	A4
PL_DDR3_RESET	IO_L16N_T2_34	A10
PL_DDR3_CLK0_P	IO_L21P_T3_DQS_34	B6
PL_DDR3_CLK0_N	IO_L21N_T3_DQS_34	A5
PL_DDR3_CKE	IO_L24P_T3_34	B2

Part 4: QSPI Flash

The AX7350B FPGA development board is equipped with a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U10	W25Q256FVEI	32M Byte	Winbond

Table 4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 4-1 shows the QSPI Flash in the schematic.

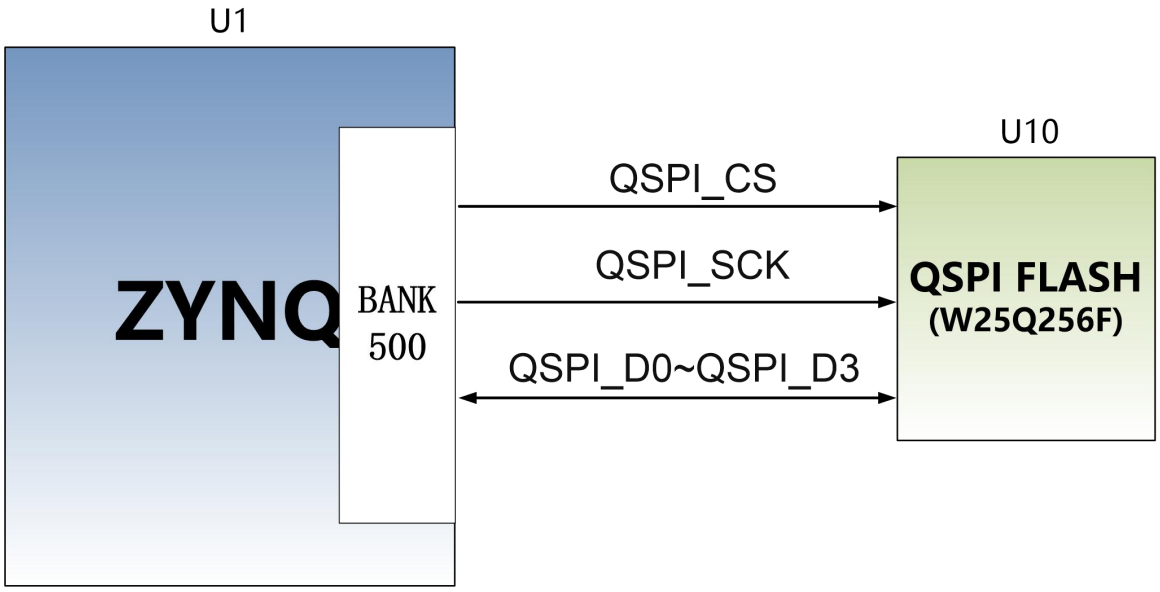


Figure 4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI_SCK	PS_MIO6_500	F23
QSPI_CS	PS_MIO1_500	D26
QSPI_D0	PS_MIO2_500	E25
QSPI_D1	PS_MIO3_500	D25
QSPI_D2	PS_MIO4_500	F24
QSPI_D3	PS_MIO5_500	C26

Part 5：eMMC Flash

The AX7350B FPGA development board is equipped with a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM applications, system files and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 5-1.

Position	Model	Capacity	Factory
U11	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 5-1: eMMC FLASH Specification

eMMC FLASH is connected to the GPIO port of the BANK501 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 5-1 shows the eMMC Flash in the schematic.

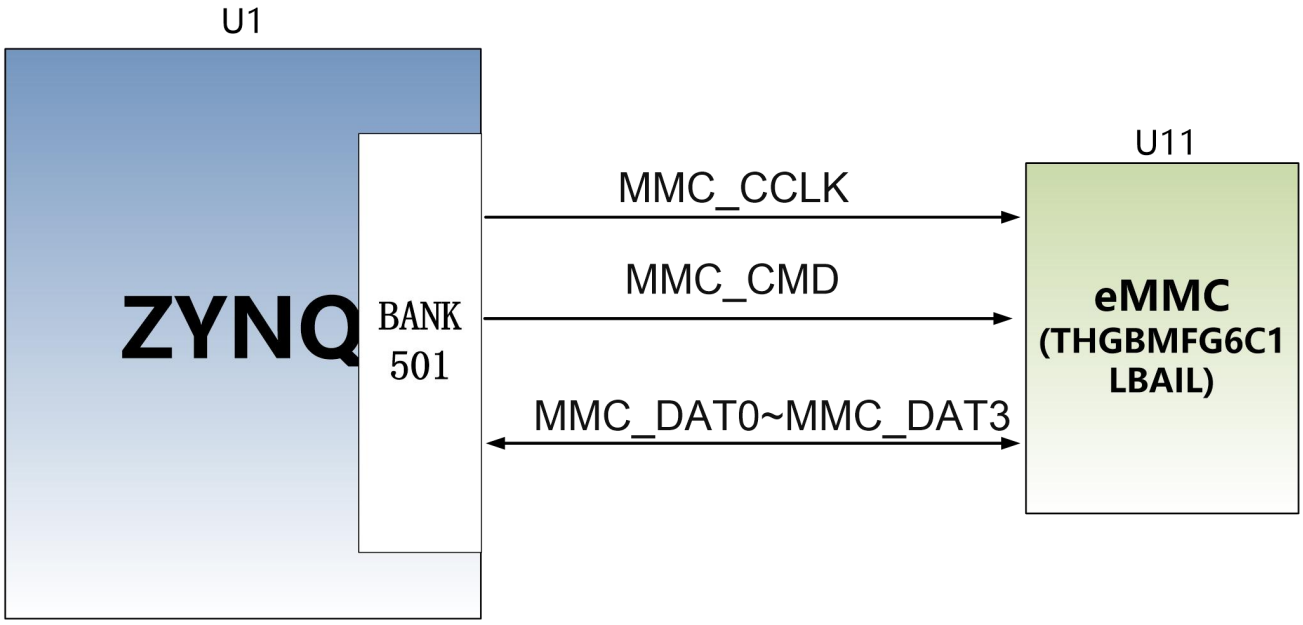


Figure 5-1: eMMC Flash in the Schematic

Pin Assignment of eMMC Flash

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
MMC_CCLK	PS_MIO48_501	B21
MMC_CMD	PS_MIO47_501	B19
MMC_D0	PS_MIO46_501	E17
MMC_D1	PS_MIO49_501	A18
MMC_D2	PS_MIO50_501	B22
MMC_D3	PS_MIO51_501	B20

Part 6: Clock Configuration

The AX7350B FPGA development board provides a single-ended active clock for the PS system and the PL logic, allowing the PS system and PL logic to work independently.

PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS section via the X4 crystal on the development board. The input of the clock is connected to the pin of the PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic

diagram is shown in Figure 6-1:

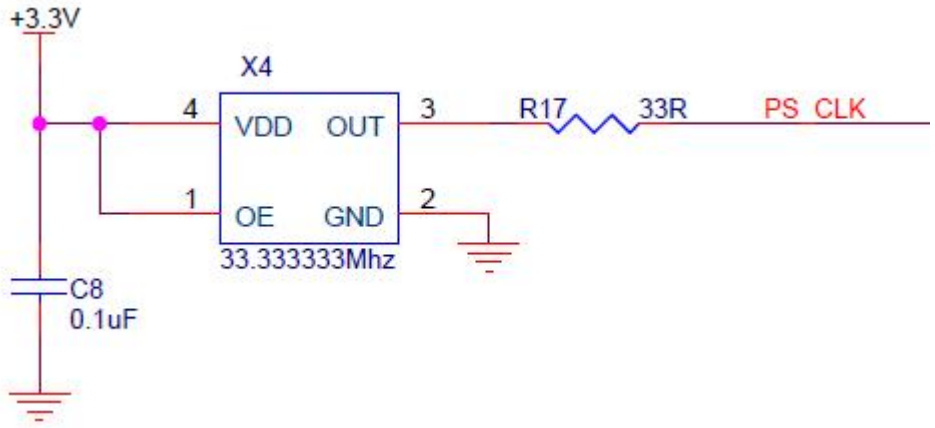


Figure 6-1: Active crystal oscillator to the PS section

PS Clock Pin Assignment

Signal Name	ZYNQ Pin
PS_CLK	B24

PL system clock source

The AX7350B development board provides a single-ended 50MHz PL system clock source with 1.8V supply. The crystal output is connected to the global clock (MRCC) of the FPGA BANK35, which can be used to drive user logic circuit within the FPGA. The schematic diagram of the clock source is shown in Figure 6-2.

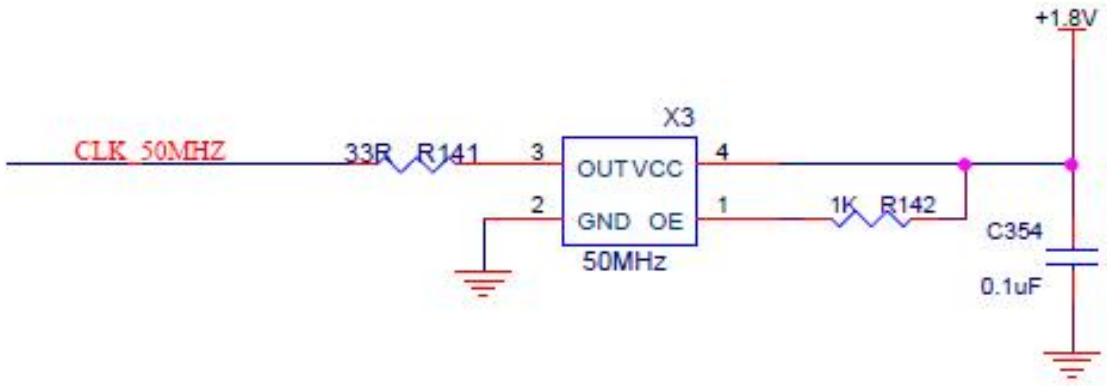


Figure 6-2: PL system clock source

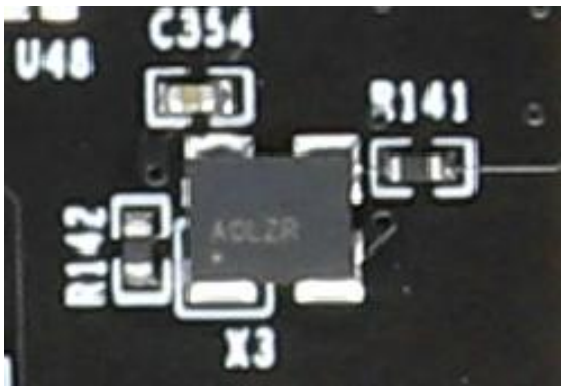


Figure 6-4: 50Mhz active crystal oscillator on the AX7350B board

PL Clock pin assignment:

Signal Name	ZYNQ Pin
CLK_50MHZ	J14

DDR Reference Clock

A 200MHz differential crystal oscillator is provided to bank34 as the reference clock of the DDR controller of PL;

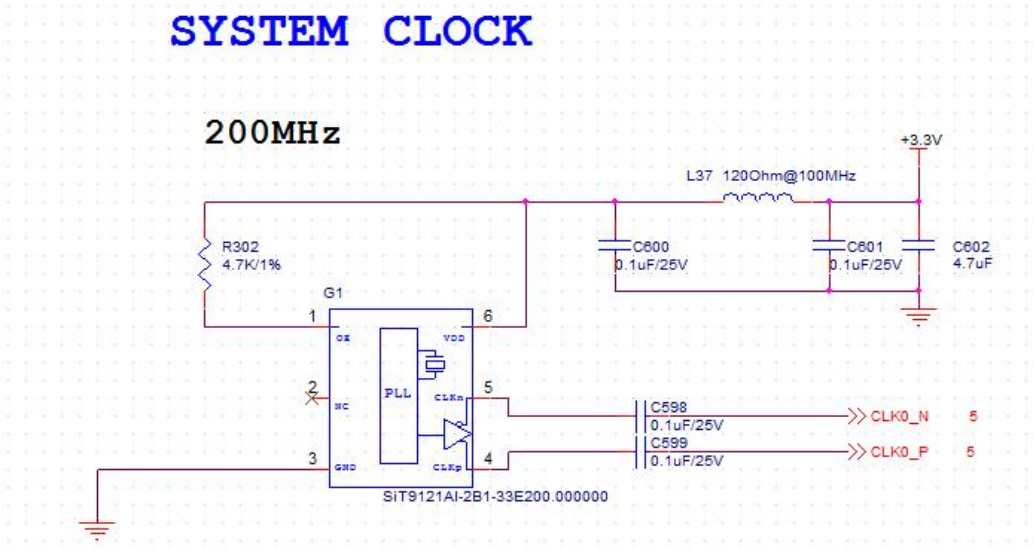


Figure 6-3 200Mhz active crystal oscillator for DDR

PL Clock Pin Assignment:

Signal Name	ZYNQ Pin
CLK0_P	C8
CLK0_N	C7

Transceiver Reference Clock

One 156mhz differential crystal oscillator is provided to bank111 as the reference clock of SPF of GTX transceiver; In addition, two channels of 100MHz differential reference clock are generated by the dsc557-0334fi1 chip and provided to the bank112 and PCIe socket respectively. The schematic diagram of the reference circuit design is shown in the following figure:

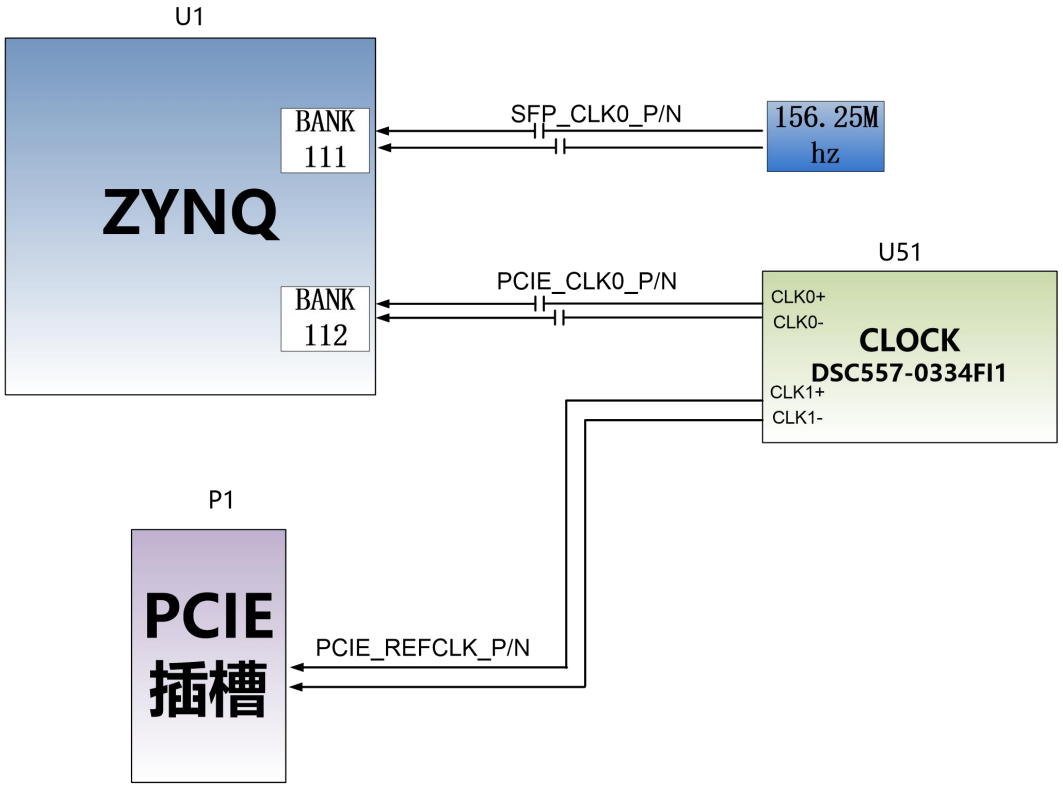


Figure 6-4 Programmable clock source

Programmable clock source ZYNQ pin assignment:：

Signal Name	ZYNQ Pin

PCIE_CLK0_P	R6
PCIE_CLK0_N	R5
SFP_CLK0_C_P	AA6
SFP_CLK0_C_N	AA5

Part 7: USB to Serial Port

The development board is equipped with a Uart to USB interface for separate power supply and debugging of the core board. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

The schematic diagram of the USB Uart circuit design is shown in Figure 7-1:

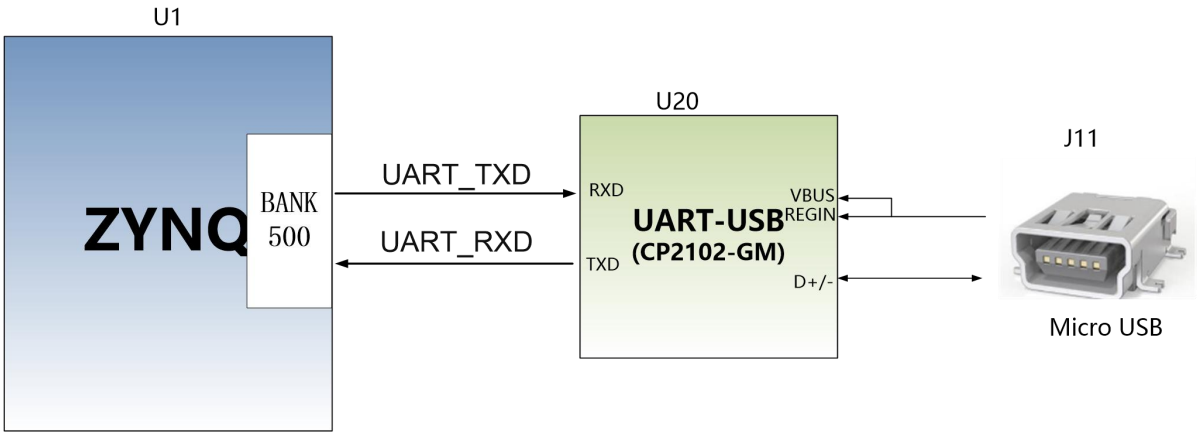


Figure 7-1: USB to serial port schematic

USB to serial port ZYNQ pin assignment:

Signal name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_RXD	PS_MIO13_500	B25	Uart data input

UART_TXD	PS_MIO12_500	A23	Uart data output

Part 8: Gigabit Ethernet Interface

The AX7350B FPGA development board has two Gigabit Ethernet interfaces, one of which is the connected PS system end, and the other one is connected to the logical IO port of the PL. The Gigabit Ethernet interface connected to the PL side needs to be mounted to the ZXIQ AXI bus system by calling the IP.

The Ethernet chip uses JLSemi JL2121-N040I Industrial Ethernet GPHY chip to provide network communication services to users. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the BANK501 of the PS side of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of the BANK35. The JL2121 chip supports 10/100/1000 Mbps network transmission rate and communicates with the MAC layer of the Zynq7000 system through the RGMII interface. JL2121 supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and supports MDIO bus for PHY register management.

The JL2121 power-on will detect the level status of some specific IOs to determine their working mode. Table 8-1 describes the default setup information after the GPHY chip is powered up.。

Configuration Pin	Instructions	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	MDIO/MDC Mode PHYaddress	PHY Address 001
RXD1_TXDLY	TX clock 2ns delay	delay
RXD0_RXDLY	RX clock 2ns delay	delay

Table 8-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock. Figure 8-1 detailed the connection of the ZYNQ PS end 1 way Ethernet PHY chip, and Figure 8-2 detailed the connection of the 1 way Ethernet PHY chip on the ZYNQ PL side:

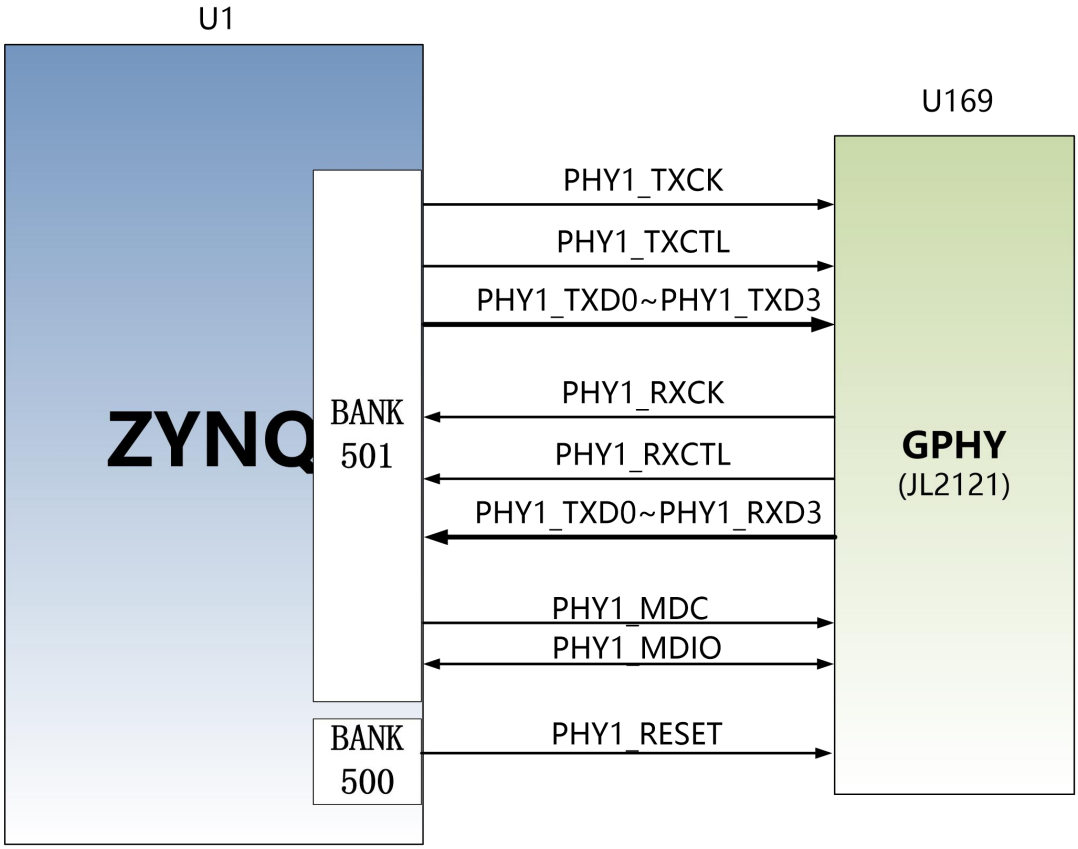


Figure 8-1: The connection of the ZYNQ PS end and GPHY chip

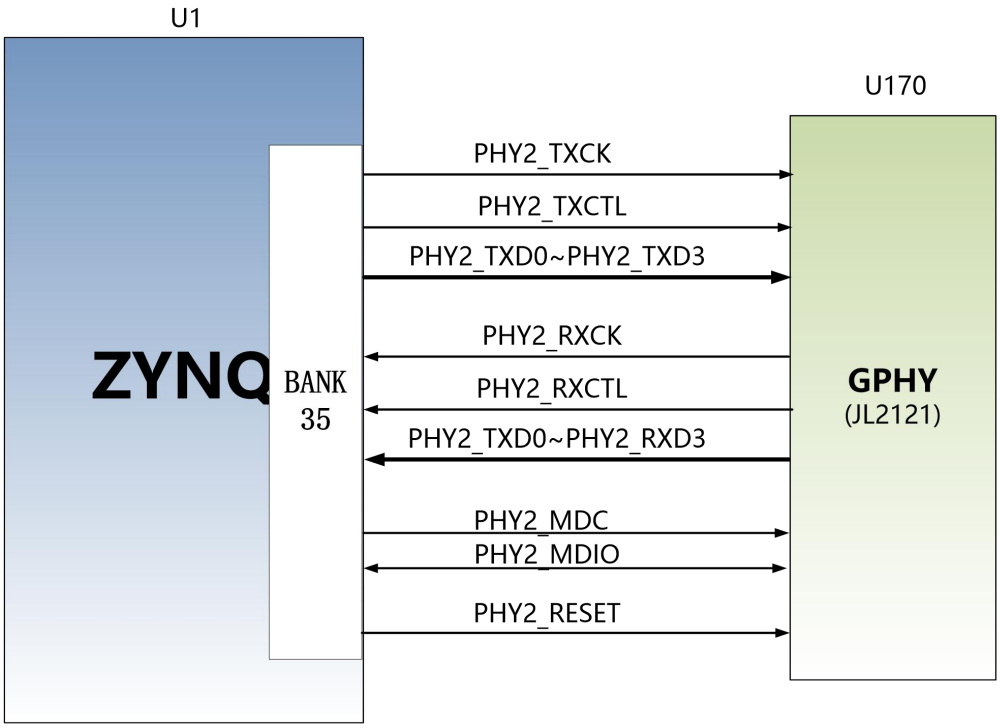


Figure 8-2: The connection of the ZYNQ PL end and GPHY chip

PS side Gigabit Ethernet pin assignments are as follows：

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY1_TXCK	PS_MIO16_501	G21	RGMII Transmit Clock
PHY1_TXD0	PS_MIO17_501	G17	Transmit data bit0
PHY1_TXD1	PS_MIO18_501	G20	Transmit data bit1
PHY1_TXD2	PS_MIO19_501	G19	Transmit data bit2
PHY1_TXD3	PS_MIO20_501	H19	Transmit data bit3
PHY1_TXCTL	PS_MIO21_501	F22	Transmit enable signal
PHY1_RXCK	PS_MIO22_501	G22	RGMII Receive Clock
PHY1_RXD0	PS_MIO23_501	F20	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	J19	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	F19	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	H17	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	F18	Receive data valid signal
PHY1_MDC	PS_MIO52_501	A20	MDIO Management clock
PHY1_MDIO	PS_MIO53_501	A19	MDIO Management data

PHY1_RESET	PS_MIO7_500	E23	Reset signal

PL-side Gigabit Ethernet pin assignments are as follows：

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY2_TXCK	IO_L4N_T0_35	D11	RGMII Transmit Clock
PHY2_TXD0	IO_L3N_T0_DQS_AD1N_35	F10	Transmit data bit0
PHY2_TXD1	IO_L3P_T0_DQS_AD1P_35	G10	Transmit data bit1
PHY2_TXD2	IO_L2N_T0_AD8N_35	D10	Transmit data bit2
PHY2_TXD3	IO_L2P_T0_AD8P_35	E10	Transmit data bit3
PHY2_TXCTL	IO_L4P_T0_35	E11	Transmit enable signal
PHY2_RXCK	IO_L11P_T1_SRCC_35	G14	RGMII Receive Clock
PHY2_RXD0	IO_L6P_T0_35	F13	Receive data Bit0
PHY2_RXD1	IO_L1P_T0_AD0P_35	F12	Receive data Bit1
PHY2_RXD2	IO_L1N_T0_AD0N_35	E12	Receive data Bit2
PHY2_RXD3	IO_L5N_T0_AD9N_35	G11	Receive data Bit3
PHY2_RXCTL	IO_L6N_T0_VREF_35	E13	Receive data valid signal
PHY2_MDC	IO_0_VRN_35	H16	MDIO Management clock
PHY2_MDIO	IO_L7P_T1_AD2P_35	H13	MDIO Management data
PHY2_RESET	IO_L7N_T1_AD2N_35	H12	Reset signal

Part 9: USB2.0 Host Interface

There are 4 USB2.0 HOST interfaces on the AX7350B FPGA development board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface, and then expands the 4-way USB HOST interfaces through a USB HUB chip USB2514. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver for high-speed USB2.0 Host mode data communication. The USB3320C's USB data and control signals are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. The USB interface differential signal (DP/DM) is connected to the USB2514 chip to extend the four USB ports. Two 24MHz crystals provide clocks for the USB3320C and USB2514 chips, respectively.

The four USB ports are flat USB ports (USB Type A), which allows users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time. Each USB interface provides +5V power.

The schematic diagram of the ZYNQ processor, USB3320C-EZK chip, USB2514 chip connection are shown as Figure 3-3-1

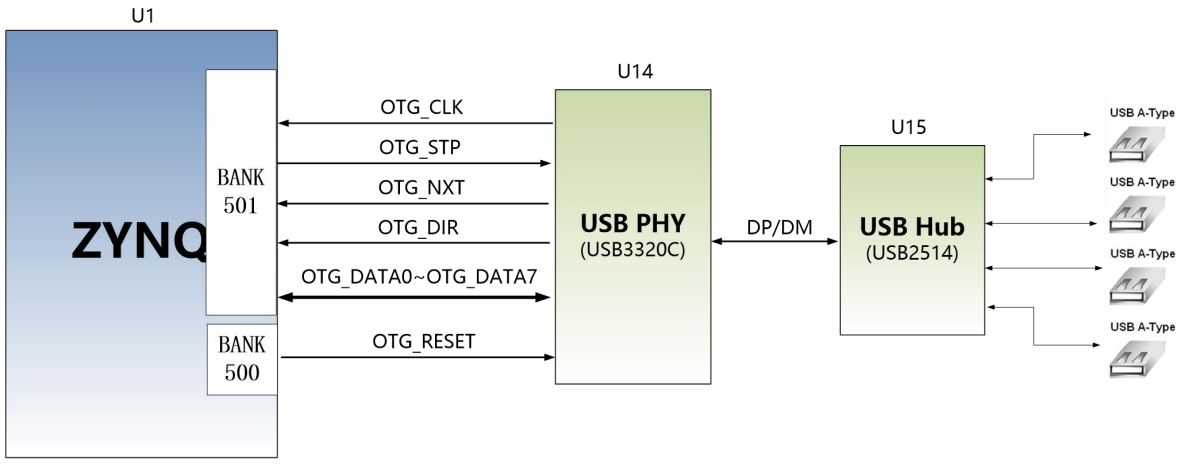


Figure 9-1: The connection between Zynq7000 and USB chip

Figure 9-2 shows the physical diagram of the USB 2.0 chip and interface, where the USB interface uses a dual USB interface.

USB2.0 Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28_501	J18	USB Data Bit4
OTG_DIR	PS_MIO29_501	E20	USB Data Direction Signal
OTG_STP	PS_MIO30_501	K19	USB Stop Signal
OTG_NXT	PS_MIO31_501	E21	USB Next Data Signal
OTG_DATA0	PS_MIO32_501	K17	USB Data Bit0
OTG_DATA1	PS_MIO33_501	E22	USB Data Bit1
OTG_DATA2	PS_MIO34_501	J16	USB Data Bit2
OTG_DATA3	PS_MIO35_501	D19	USB Data Bit3
OTG_CLK	PS_MIO36_501	K16	USB Clock Signal
OTG_DATA5	PS_MIO37_501	D20	USB Data Bit5
OTG_DATA6	PS_MIO38_501	D21	USB Data Bit6
OTG_DATA7	PS_MIO39_501	C21	USB Data Bit7

OTG_RESETN	PS_MIO8_500	A24	USB Reset Signal

Part 10: HDMI Output Interface

The implementation of HDMI output interface is ADALOG DEVICE's ADV7511 HDMI (DVI) encoding chip, which supports 1080P@60Hz output and supports 3D output.

Among them, the ADV7511's video digital interface, audio digital interface and I2C configuration interface are connected with the BANK35 IO of the ZYNQ7000 PL part. The ZYNQ7000 system initializes and controls the ADV7511 through the I2C pin. The hardware connection diagram of ADV7511 chip and ZYNQ7000 is shown in Figure 10-1.

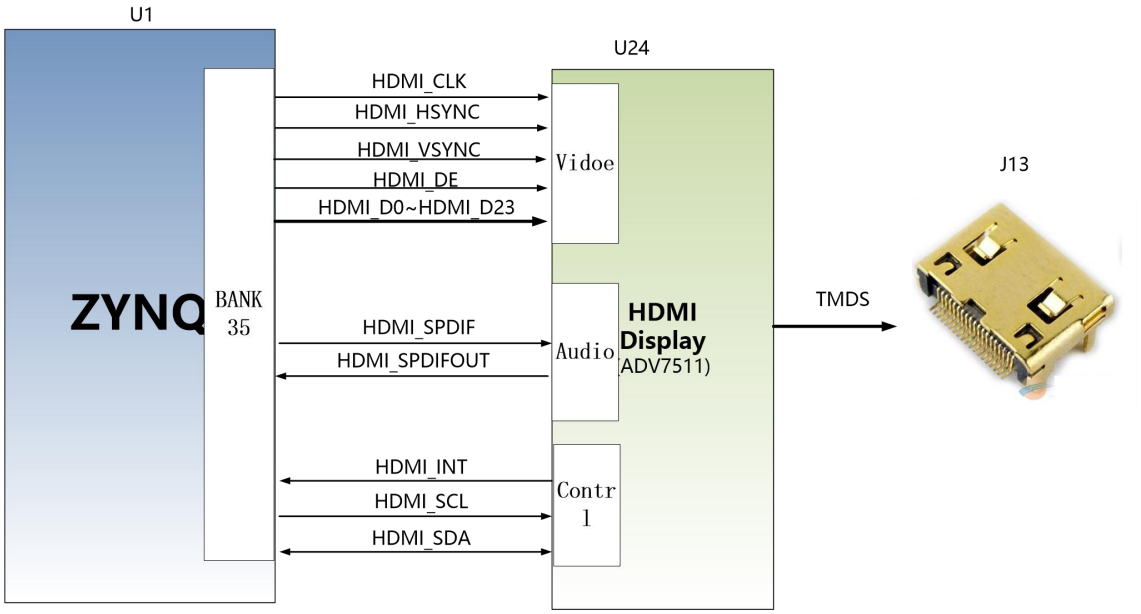


Figure 10-1: HDMI interface design schematic

ZYNQ Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
HDMI_CLK	IO_L8P_T1_AD10P_35	K13	HDMI Video signal clock
HDMI_HSYNC	IO_L23P_T3_35	C11	HDMI Video signal line synchronization

HDMI_VSYNC	IO_L22N_T3_AD7N_35	B12	HDMI Video signal column synchronization
HDMI_DE	IO_L9P_T1_DQS_AD3P_35	K15	HDMI video signal is valid
HDMI_D0	IO_L10P_T1_AD11P_35	G16	HDMI Video signal data0
HDMI_D1	IO_L16P_T2_35	E16	HDMI Video signal data1
HDMI_D2	IO_L9N_T1_DQS_AD3N_35	J15	HDMI Video signal data2
HDMI_D3	IO_L14N_T2_AD4N_SRCC_35	E15	HDMI Video signal data3
HDMI_D4	IO_L14P_T2_AD4P_SRCC_35	F15	HDMI Video signal data4
HDMI_D5	IO_L10N_T1_AD11N_35	G15	HDMI Video signal data5
HDMI_D6	IO_L11N_T1_SRCC_35	F14	HDMI Video signal data6
HDMI_D7	IO_L12N_T1_MRCC_35	H14	HDMI Video signal data7
HDMI_D8	IO_L8N_T1_AD10N_35	J13	HDMI Video signal data8
HDMI_D9	IO_25_VRP_35	K12	HDMI Video signal data9
HDMI_D10	IO_L23N_T3_35	B11	HDMI Video signal data10
HDMI_D11	IO_L22P_T3_AD7P_35	C12	HDMI Video signal data11
HDMI_D12	IO_L19P_T3_35	D13	HDMI Video signal data12
HDMI_D13	IO_L24N_T3_AD15N_35	A12	HDMI Video signal data13
HDMI_D14	IO_L19N_T3_VREF_35	C13	HDMI Video signal data14
HDMI_D15	IO_L24P_T3_AD15P_35	A13	HDMI Video signal data15
HDMI_D16	IO_L13N_T2_MRCC_35	D14	HDMI Video signal data16
HDMI_D17	IO_L13P_T2_MRCC_35	D15	HDMI Video signal data17
HDMI_D18	IO_L21N_T3_DQS_AD14N_35	A14	HDMI Video signal data18
HDMI_D19	IO_L20N_T3_AD6N_35	B14	HDMI Video signal data19
HDMI_D20	IO_L21P_T3_DQS_AD14P_35	A15	HDMI Video signal data20
HDMI_D21	IO_L17N_T2_AD5N_35	B15	HDMI Video signal data21
HDMI_D22	IO_L16N_T2_35	D16	HDMI Video signal data22
HDMI_D23	IO_L17P_T2_AD5P_35	B16	HDMI Video signal data23
HDMI_SPDIF	IO_L20P_T3_AD6P_35	C14	HDMI Audio S/PDIF Input
HDMI_SPDIFOUT	IO_L18P_T2_AD13P_35	B17	HDMI Audio S/PDIF Output
HDMI_INT	IO_L15P_T2_DQS_AD12P_35	C17	HDMI Interrupt signal
HDMI_SCL	IO_L18N_T2_AD13N_35	A17	HDMI IIC Control clock
HDMI _SDA	IO_L15N_T2_DQS_AD12N_35	C16	HDMI IIC Control data

Part 11: SFP Interface

The AX7350B FPGA development board has two optical interfaces. Users

can purchase SFP optical modules (1.25G, 2.5G, 10G optical modules on the market) and insert them into these two optical interfaces for optical data communication. The 2-way fiber interface is connected to the 2-way RX/TX of the ZNKQ's BANK111 GTX transceiver. Both the TX signal and the RX signal are connected to the ZYNQ and the optical module through a DC blocking capacitor in a differential signal mode, and each TX transmission and RX reception data rate is up to 10 Gb/s. The reference clock for the BANK111 GTX transceiver is provided by 156.25Mhz Differential crystal oscillator.

Figure 11-1 detailed the FPGA and SFP schematic diagram

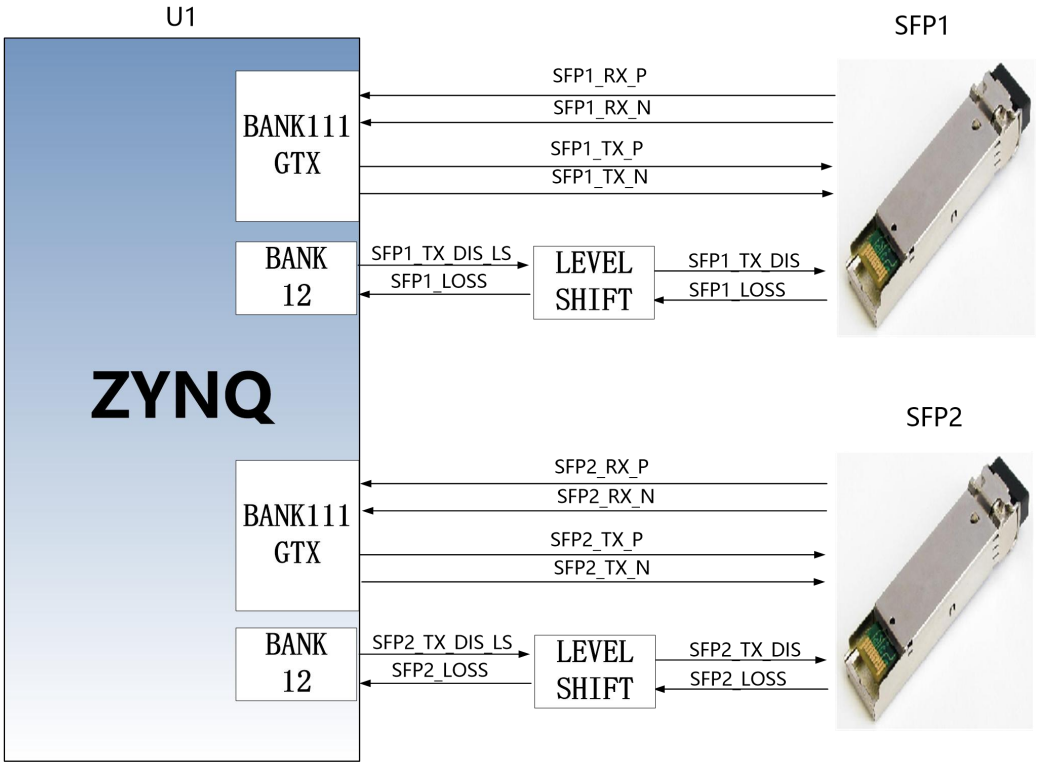


Figure 11-1: The schematic diagram of FPGA and Fiber Interface

The first fiber interface ZYNQ pin assignment is as follows:

Signal Name	ZYNQ Pin	Description
SFP1_TX_P	AF4	SFP Module Data Transmission Positive
SFP1_TX_N	AF3	SFP Module Data Transmission Negative
SFP1_RX_P	AE6	SFP Module Data Receive Positive
SFP1_RX_P	AE5	SFP Module Data Receive Negative

SFP1_TX_DIS_LS	AA14	SFP Module Transmission Prohibition High Level Active
SFP1_LOSS_LS	W16	SFP Receives LOSS signal, High Indicates No optical signal received

The Second fiber interface ZYNQ pin assignment is as follows:

Signal Name	ZYNQ Pin	Description
SFP2_TX_P	AE2	SFP Module Data Transmission Positive
SFP2_TX_N	AE1	SFP Module Data Transmission Negative
SFP2_RX_P	AC6	SFP Module Data Receive Positive
SFP2_RX_P	AC5	SFP Module Data Receive Negative
SFP2_TX_DIS_LS	Y16	SFP Module Transmission Prohibition High Level Active
SFP2_LOSS_LS	W15	SFP Receives LOSS signal, High Indicates No optical signal received

Part 12: PCIe Slot

The AX7350B FPGA development board has a PCIe x8 slot that physically connects to the PCIe board. In the electrical connection, we only have 4 pairs of transceivers connected to the PCIEx8 slot, so only PCIEex4, PCIex2, PCIex1 data communication can be realized.

The transmit and receive signals of the PCIe interface are directly connected to the GTX transceiver of the ZYNQ BANK112. The four TX signals and the RX signals are connected to the BANK112 by differential signals, and the single-channel communication rate can be up to 5G bit bandwidth. The reference clock of the PCIe slot is provided by the clock chip SI5338P with a reference clock frequency of 100Mhz.

The PCIe interface design diagram of the FPGA development board is shown in Figure 12-1, where the TX transmission signal is connected in AC coupling mode.

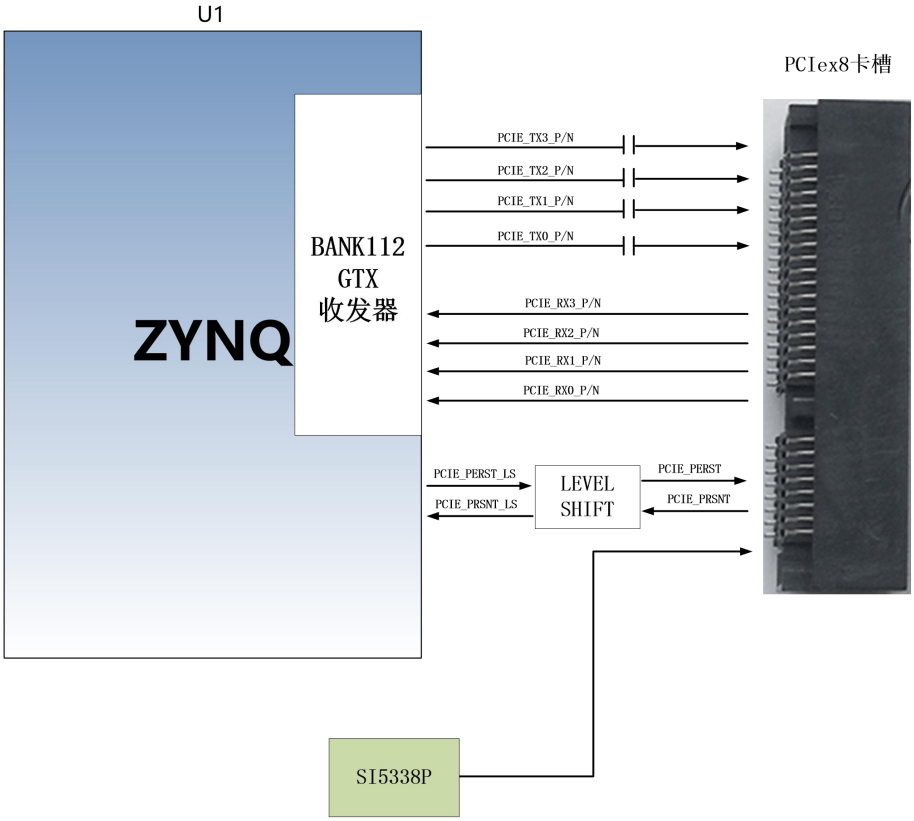


Figure 12-1: PCIe slot design schematic

PCIe x4 Interface Pin Assignment:

Signal Name	FPGA Pin	Description
PCIE_RX0_P	AB4	PCIE Channel 0 Data Receive Positive
PCIE_RX0_N	AB3	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	Y4	PCIE Channel 1 Data Receive Positive
PCIE_RX1_N	Y3	PCIE Channel 1 Data Receive Negative
PCIE_RX2_P	V4	PCIE Channel 2 Data Receive Positive
PCIE_RX2_N	V3	PCIE Channel 2 Data Receive Negative
PCIE_RX3_P	T4	PCIE Channel 3 Data Receive Positive
PCIE_RX3_N	T3	PCIE Channel 3 Data Receive Negative
PCIE_TX0_P	AA2	PCIE Channel 0 Data Transmit Positive
PCIE_TX0_N	AA1	PCIE Channel 0 Data Transmit Negative
PCIE_TX1_P	W2	PCIE Channel 1 Data Transmit Positive
PCIE_TX1_N	W1	PCIE Channel 1 Data Transmit Negative
PCIE_TX2_P	U2	PCIE Channel 2 Data Transmit Positive
PCIE_TX2_N	U1	PCIE Channel 2 Data Transmit Negative
PCIE_TX3_P	R2	PCIE Channel 3 Data Transmit Positive

PCIE_TX3_N	R1	PCIE Channel 3 Data Transmit Negative
PCIE_PERST_LS	AA19	PCIE board reset signal
PCIE_PRSNT_LS	AA18	PCIE board presence indicator

Part 13: SD Card Slot

The AX7350B FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 13-1:

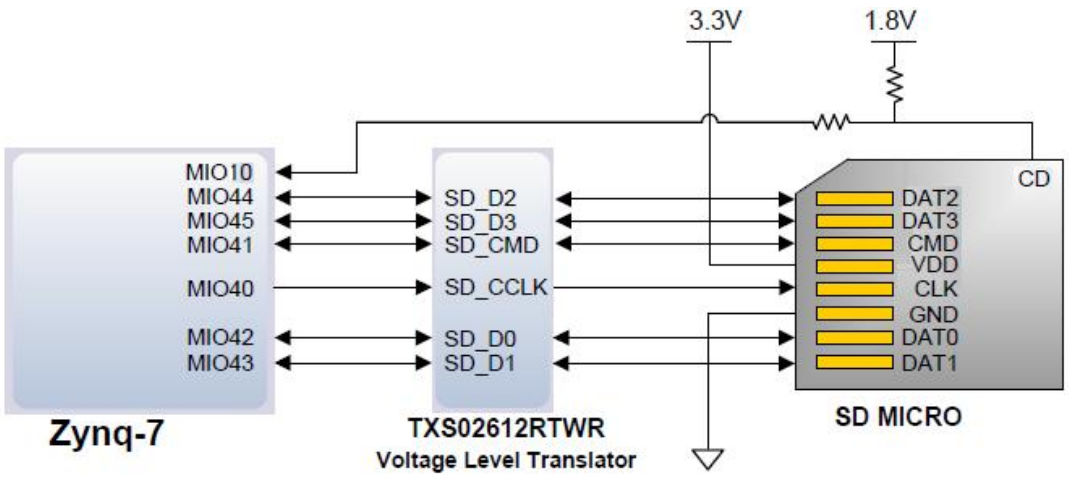


Figure 13-1: SD Card Connection Diagram

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description

SD_CLK	PS_MIO40	C22	SD Clock Signal
SD_CMD	PS_MIO41	C19	SD Command Signal
SD_D0	PS_MIO42	F17	SD Data0
SD_D1	PS_MIO43	D18	SD Data1
SD_D2	PS_MIO44	E18	SD Data2
SD_D3	PS_MIO45	C18	SD Data3
SD_CD	PS_MIO10	A25	SD Card Insertion Signal

Part 14: FMC Connector

The AX7350B FPGA development board has a standard FMC LPC expansion port that can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 34 pairs of differential IO signals and one high-speed GTX transceiver signal.

The 33 pairs of differential signals of the FMC expansion port are connected to the IOs of the BANK12 and BANK13 of the ZYNQ chip. The IO level standard of BANK12 and BANK13 is determined by the voltage VADJ of BANK. The default is 2.5V, which enables 34 pairs of differential signals to support LVDS data communication. The other GTX transceiver signal and reference clock signal are connected to the GTX transceiver and clock input of the ZYNQ BANK111, respectively. The schematic diagram of the Zynq7000 and FMC connectors is shown in Figure 14-1.

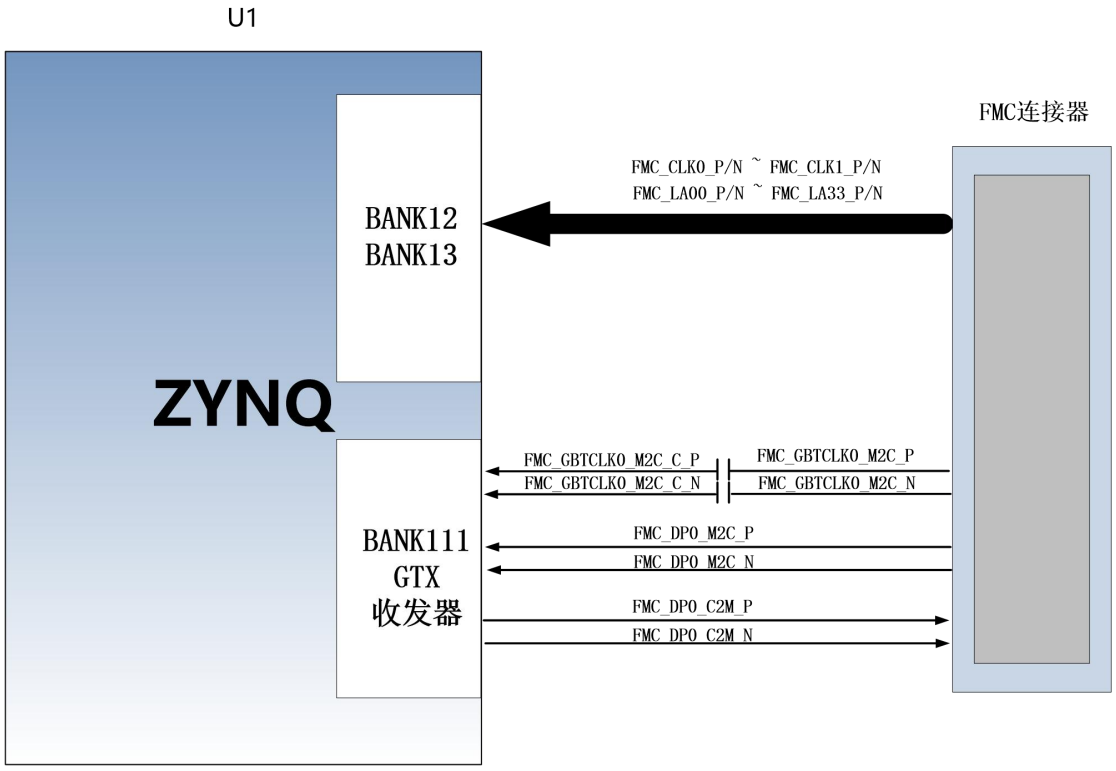


Figure 14-1: FMC connection diagram

FMC connector pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
FMC_CLK0_P	IO_L12P_T1_MRCC_12	AC13	FMC reference 1st channel reference clock P
FMC_CLK0_N	IO_L12N_T1_MRCC_12	AD13	FMC reference 1st channel reference clock N
FMC_CLK1_P	IO_L13P_T2_MRCC_13	AD20	FMC reference 2nd channel reference clock P
FMC_CLK1_N	IO_L13N_T2_MRCC_13	AD21	FMC reference 2nd channel reference clock N
FMC_LA00_CC_P	IO_L13P_T2_MRCC_12	AC14	FMC reference 0th channel data (clock)P
FMC_LA00_CC_N	IO_L13N_T2_MRCC_12	AD14	FMC reference 0th channel data (clock)N
FMC_LA01_CC_P	IO_L14P_T2_SRCC_12	AB15	FMC reference 1st channel data (clock) P
FMC_LA01_CC_N	IO_L14N_T2_SRCC_12	AB14	FMC reference 1st channel data (clock) N

FMC_LA02_P	IO_L3P_T0_DQS_12	Y10	FMC reference 2nd channel data P
FMC_LA02_N	IO_L3N_T0_DQS_12	AA10	FMC reference 2nd channel data N
FMC_LA03_P	IO_L17P_T2_12	AE16	FMC reference 3rd channel data P
FMC_LA03_N	IO_L17N_T2_12	AE15	FMC reference 3rd channel data N
FMC_LA04_P	IO_L7P_T1_12	AE10	FMC reference 4th channel data P
FMC_LA04_N	IO_L7N_T1_12	AD10	FMC reference 4th channel data N
FMC_LA05_P	IO_L11P_T1_SRCC_12	AC12	FMC reference 5th channel data P
FMC_LA05_N	IO_L11N_T1_SRCC_12	AD11	FMC reference 5th channel data N
FMC_LA06_P	IO_L9P_T1_DQS_12	AE11	FMC reference 6th channel data P
FMC_LA06_N	IO_L9N_T1_DQS_12	AF10	FMC reference 6th channel data N
FMC_LA07_P	IO_L4P_T0_12	AB11	FMC reference 7th channel data P
FMC_LA07_N	IO_L4N_T0_12	AB10	FMC reference 7th channel data N
FMC_LA08_P	IO_L1P_T0_12	Y12	FMC reference 8th channel data P
FMC_LA08_N	IO_L1N_T0_12	Y11	FMC reference 8th channel data N
FMC_LA09_P	IO_L10P_T1_12	AE13	FMC reference 9th channel data P
FMC_LA09_N	IO_L10N_T1_12	AF13	FMC reference 9th channel data N
FMC_LA10_P	IO_L2P_T0_12	AB12	FMC reference 10th channel data P
FMC_LA10_N	IO_L2N_T0_12	AC11	FMC reference 10th channel data N
FMC_LA11_P	IO_L8P_T1_12	AE12	FMC reference 11th channel data P
FMC_LA11_N	IO_L8N_T1_12	AF12	FMC reference 11th channel data N
FMC_LA12_P	IO_L5P_T0_12	W13	FMC reference 12th channel data P
FMC_LA12_N	IO_L5N_T0_12	Y13	FMC reference 12th channel data N
FMC_LA13_P	IO_L15P_T2_DQS_12	AD16	FMC reference 13th channel data P
FMC_LA13_N	IO_L15N_T2_DQS_12	AD15	FMC reference 13th channel data N
FMC_LA14_P	IO_L16P_T2_12	AF15	FMC reference 14th channel data P
FMC_LA14_N	IO_L16N_T2_12	AF14	FMC reference 14th channel data N
FMC_LA15_P	IO_L18P_T2_12	AE17	FMC reference 15th channel data P
FMC_LA15_N	IO_L18N_T2_12	AF17	FMC reference 15th channel data N
FMC_LA16_P	IO_L20P_T3_12	AB17	FMC reference 16th channel data P
FMC_LA16_N	IO_L20N_T3_12	AB16	FMC reference 16th channel data N
FMC_LA17_CC_P	IO_L12P_T1_MRCC_13	AC23	FMC reference 17th channel data (clock) P
FMC_LA17_CC_N	IO_L12N_T1_MRCC_13	AC24	FMC reference 17th channel data (clock) N
FMC_LA18_CC_P	IO_L11P_T1_SRCC_13	AD23	FMC reference 18th channel data (clock) P

FMC_LA18_CC_N	IO_L11N_T1_SRCC_13	AD24	FMC reference 18th channel data (clock) N
FMC_LA19_P	IO_L16P_T2_13	AE20	FMC reference 19th channel data P
FMC_LA19_N	IO_L16N_T2_13	AE21	FMC reference 19th channel data N
FMC_LA20_P	IO_L15P_T2_DQS_13	AF19	FMC reference 20th channel data P
FMC_LA20_N	IO_L15N_T2_DQS_13	AF20	FMC reference 20th channel data N
FMC_LA21_P	IO_L20P_T3_13	AA20	FMC reference 21st channel data P
FMC_LA21_N	IO_L20N_T3_13	AB20	FMC reference 21st channel data N
FMC_LA22_P	IO_L17P_T2_13	AD18	FMC reference 22nd channel data P
FMC_LA22_N	IO_L17N_T2_13	AD19	FMC reference 22nd channel data N
FMC_LA23_P	IO_L18P_T2_13	AE18	FMC reference 23rd channel data P
FMC_LA23_N	IO_L18N_T2_13	AF18	FMC reference 23rd channel data N
FMC_LA24_P	IO_L8P_T1_13	AE23	FMC reference 27th channel data P
FMC_LA24_N	IO_L8N_T1_13	AF23	FMC reference 24th channel data N
FMC_LA25_P	IO_L9P_T1_DQS_13	AB21	FMC reference 25th channel data P
FMC_LA25_N	IO_L9N_T1_DQS_13	AB22	FMC reference 25th channel data N
FMC_LA26_P	IO_L7P_T1_13	AE22	FMC reference 27th channel data P
FMC_LA26_N	IO_L7N_T1_13	AF22	FMC reference 26th channel data N
FMC_LA27_P	IO_L14P_T2_SRCC_13	AC21	FMC reference 27th channel data P
FMC_LA27_N	IO_L14N_T2_SRCC_13	AC22	FMC reference 27th channel data N
FMC_LA28_P	IO_L10P_T1_13	AA22	FMC reference 29th channel data P
FMC_LA28_N	IO_L10N_T1_13	AA23	FMC reference 28th channel data N
FMC_LA29_P	IO_L5P_T0_13	AF24	FMC reference 29th channel data P
FMC_LA29_N	IO_L5N_T0_13	AF25	FMC reference 29th channel data N
FMC_LA30_P	IO_L4P_T0_13	AD25	FMC reference 30th channel data P
FMC_LA30_N	IO_L4N_T0_13	AD26	FMC reference 30th channel data N
FMC_LA31_P	IO_L3P_T0_DQS_13	AE25	FMC reference 31st channel data P
FMC_LA31_N	IO_L3N_T0_DQS_13	AE26	FMC reference 31st channel data N
FMC_LA32_P	IO_L2P_T0_13	AB26	FMC reference 32nd channel data P
FMC_LA32_N	IO_L2N_T0_13	AC26	FMC reference 32nd channel data N
FMC_LA33_P	IO_L1P_T0_13	AA25	FMC reference 33rd data P
FMC_LA33_N	IO_L1N_T0_13	AB25	FMC reference 33rd data N

Part 15: LED Light

The AX7350B FPGA development board has 9 LEDs, 1 power indicator; 1 DONE configuration indicator; 2 serial communication indicators, 1 PS control LED, and 4 PL control indicators. The power indicator will illuminate when the board is powered on; the configuration LED will illuminate when the FPGA is configured. One user LED light is connected to the MIO of the PS, and four LED lights are connected to the IO of the PL. The user can control the lighting and extinguishing through the program. When the IO voltage connected to the user LED is low, the user LED is off, and when the connection IO voltage is high, the user LED is illuminated. Since the level of BANK34 is 1.5V, here we have added a Transistor to drive the LED on and off. Figure 15-1 detailed the LED light hardware connection diagram

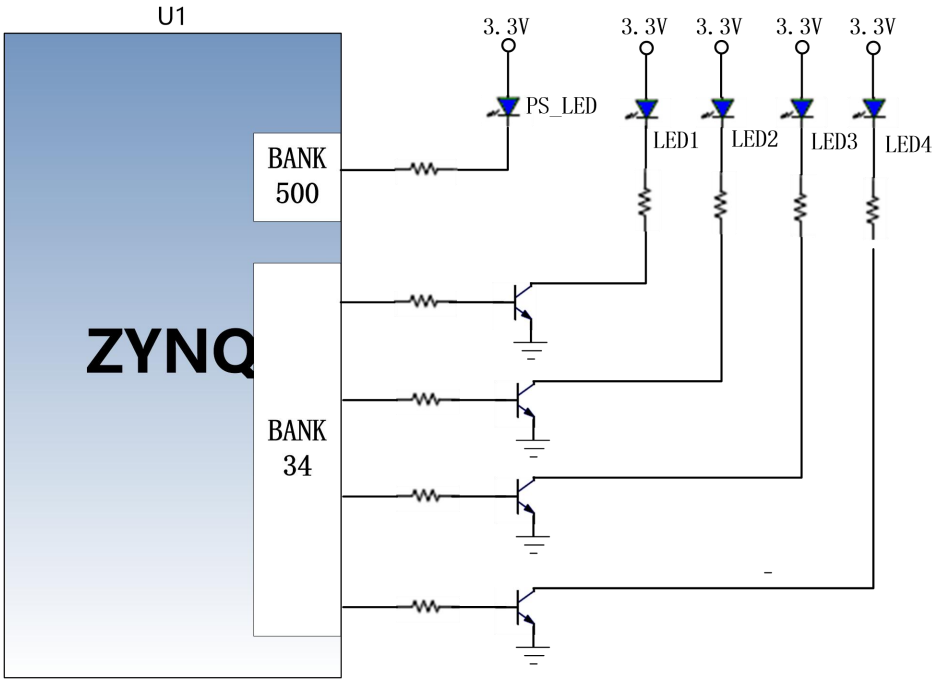


Figure 15-1: The User LEDs Hardware Connection Diagram

Pin assignment of user LED lights

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
MIO0_LED	PS_MIO0_500	E26	PS User LED

PL_LED1	IO_L7P_T1_34	F5	PL User LED1
PL_LED2	IO_L7N_T1_34	E5	PL User LED2
PL_LED3	O_L2N_T0_34	G5	PL User LED3
PL_LED4	IO_L2P_T0_34	G6	PL User LED4

Part 16: Reset Button and User Button

The AX7350B FPGA development board has one reset button RESET and five user buttons. The reset signal is connected to the PS reset pin of the ZYNQ chip. The user can use this reset button to reset the ZYNQ system. One of the five user buttons is connected to the IO of the PS, and the other four buttons are connected to the IO of the PL. . The reset button and the user button are all active low. The connection between the reset button and the user button is shown in Figure 16-1.

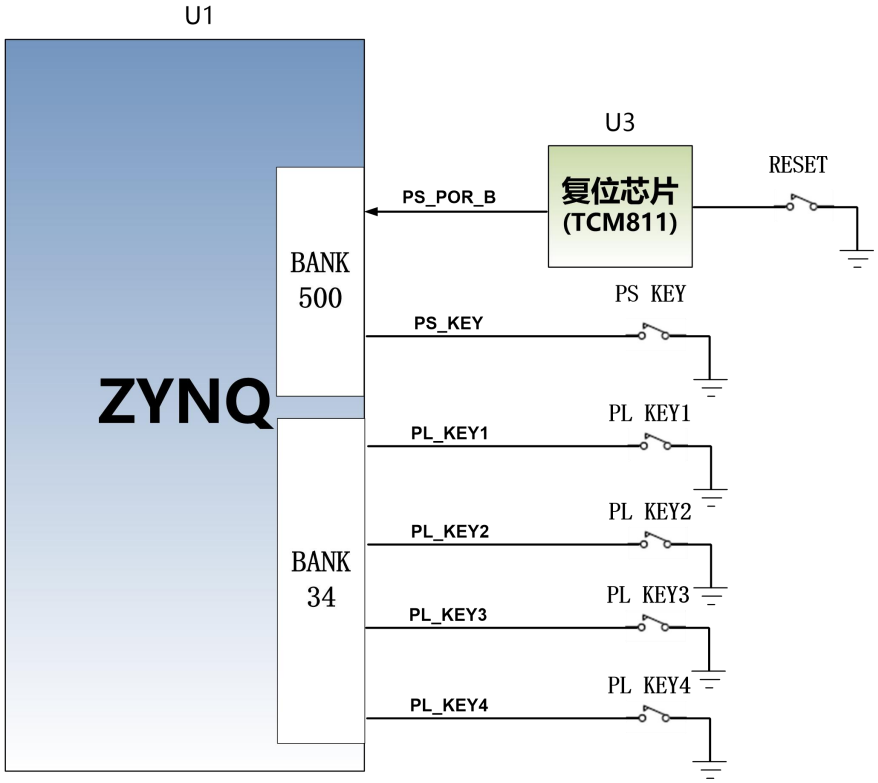


Figure 16-1: Buttons Connection Diagram

ZYNQ pin assignment of the button

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B_500	C23	ZYNQ System Reset Signal
PS_KEY	PS_MIO11_500	B26	PS button input
PL_KEY1	IO_L4N_T0_34	H6	PL button 1 input
PL_KEY2	IO_L4P_T0_34	H7	PL button 2 input
PL_KEY3	IO_L6N_T0_VREF_34	H8	PL button 3 input
PL_KEY4	IO_L6P_T0_34	J8	PL button 4 input

Part17: JTAG Debug Port

The AX7350B FPGA development board integrates the JTAG download debug circuitry so users do not need to purchase additional Xilinx downloader. With a USB cable, you can develop and debug ZYNQ. On the AX7350B FPGA development board, a FTDI USB bridge chip FT232HL is used to realize USB of PC and JTAG debug signals TCK, TDO, TMS, TDI of ZYNQ for data communication.

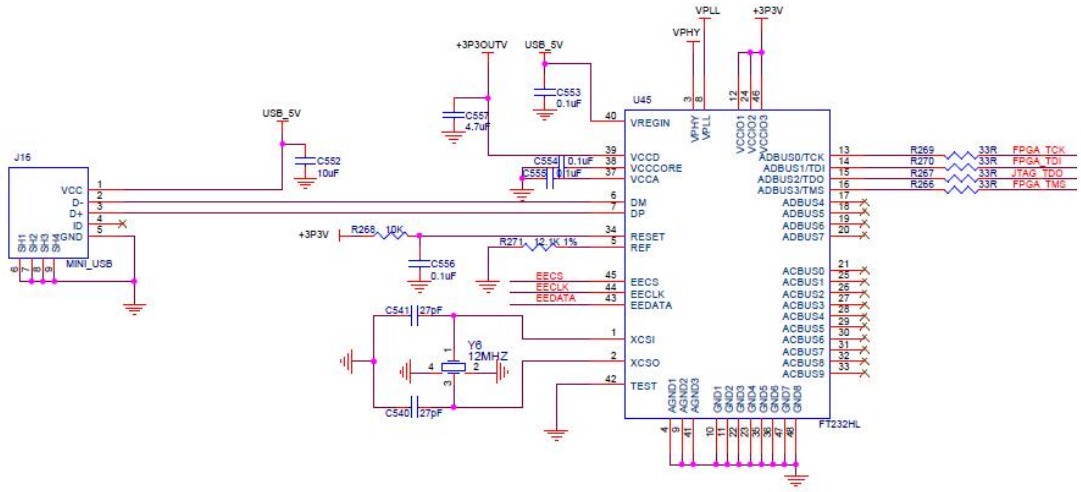


Figure 17-1: JTAG Interface Schematic

On the AX7350B FPGA development board, the JTAG interface is in the form of USB interface. Users can connect the PC and JTAG interface to the

ZYNQ system debugging through the USB cable provided by us.

Part 18: DIP Switch Configuration

The AX7350B FPGA development board has a 2-bit DIP switch SW1 to configure the ZYNQ system's startup mode. The AX7350B system development platform supports three boot modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the XC7Z035 chip is powered on, it will detect the level of the corresponding MIO port (MIO5 and MIO4) to determine which startup mode. The user can select different startup modes through the DIP switch SW1 on the board. The SW1 startup mode configuration is shown in Table 18-1.

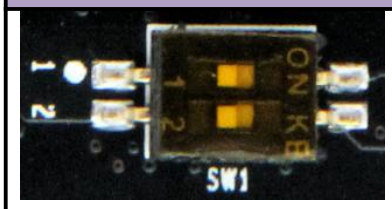
SW1	Switch Position（1，2）	MIO5,MIO4 Level	Start Mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 18-1: SW1 start mode configuration

Part 19: Power Supply

The power input voltage of the development board is DC12V, and the external +12V power supply supplies power to the board. The +12V input power supply generates +1.0V ZYNQ core power through the DCDC power chip MYMGK1R820ERSR. The MYMGK1R820ERSR output current is up to 20A, which is far enough to meet the current demand of the ZYNQ core voltage. In addition, +12V generates +1.5V through the DC/DC power chip ETA8156FT2G, and generates other power sources through the DCDC chip ETA1471FT2G. The VTT and VREF voltages of DDR3 are generated by the TPS51200 chip.

The schematic diagram of the power supply design on the AX7350B FPGA development board is shown in Figure 19-1

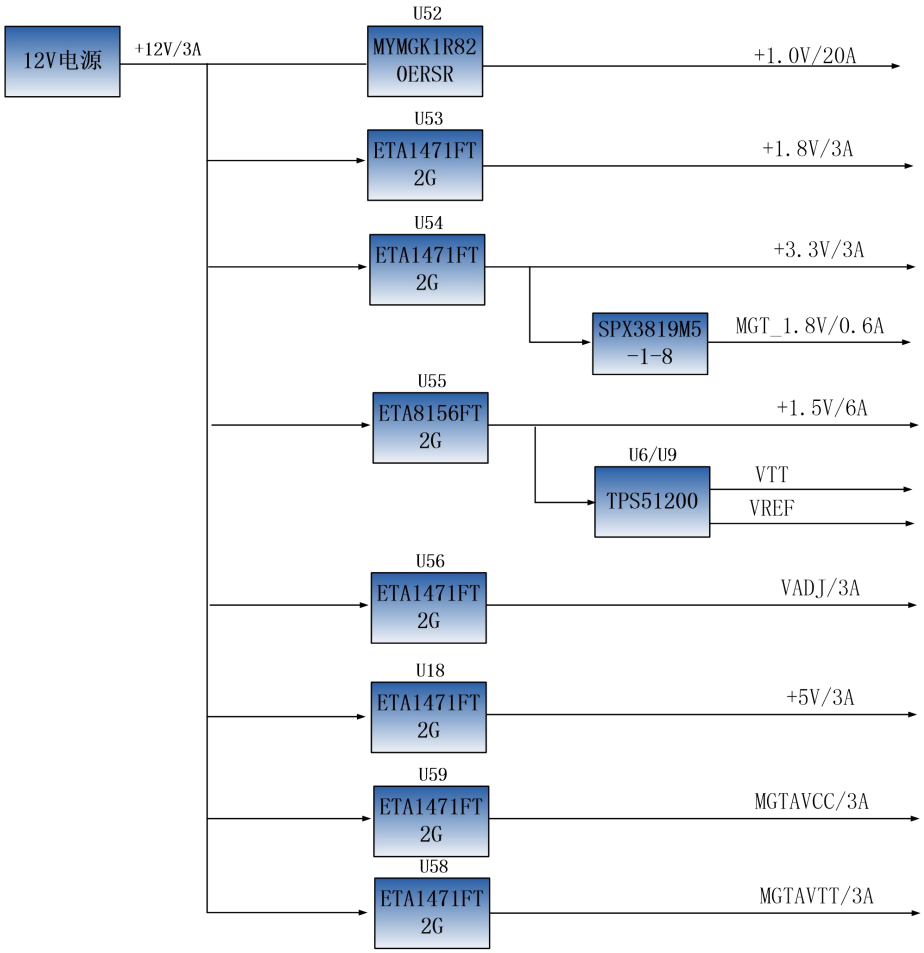


Figure 19-1: Power interface section in the schematic

The functions of each power distribution are shown in the following table:：

Power Supply	Function
+1.0V	ZYNQ PS and PL section Core Voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage,BANK501 IO Voltage，eMMC，HDMI
+3.3V	ZYNQ Bank0,Bank500，QSIP FLASH, Clock Crystal, SD Card，SFP optical module
+1.5V	DDR3, ZYNQ Bank501, Bank33,Bank34,
+1.2V	Gigabit Ethernet
VADJ(+2.5V)	ZYNQ Bank12, Bank13, FMC
VREF, VTT（+0.75V）	PS DDR3，PL DDR3

MGTAVCC(+1.0V)	ZYNQ Bank111, Bank112
MGTAVTT(+1.2V)	ZYNQ Bank111, Bank112

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO) circuit design to ensure the normal operation of the chip.

Part 20: Fan

Because ZYNQ035 generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the ZYNQ chip. The control pin is connected to the IO of the BANK34. If the IO level output is low, the MOSFET is turned on and the fan is working. If the IO level output is high, the fan stops. The fan design on the board is shown in Figure 20-1.

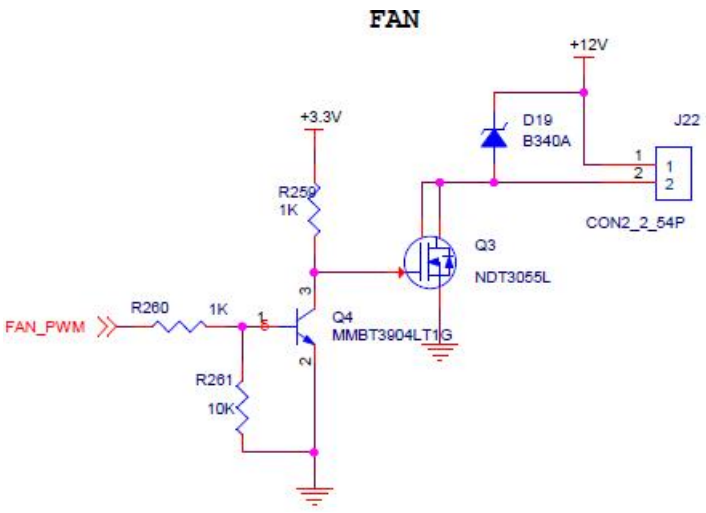


Figure 20-1：Fan design in the AX7350B FPGA Board schematic

The fan has been screwed to the AX7350B FPGA development board before leaving the factory. The power of the fan is connected to the socket of

J22. The red is positive and the black is negative. Figure 20-2 shows the physical diagram of the fan on AX7350B FPGA development board.

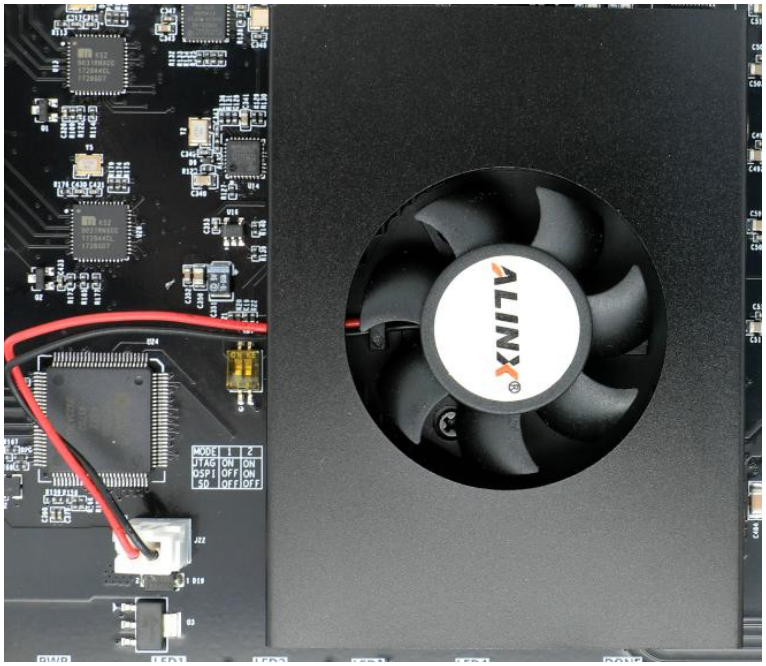


Figure 20-2: Fan on the AX7350B board

Part 21: Dimensional structure

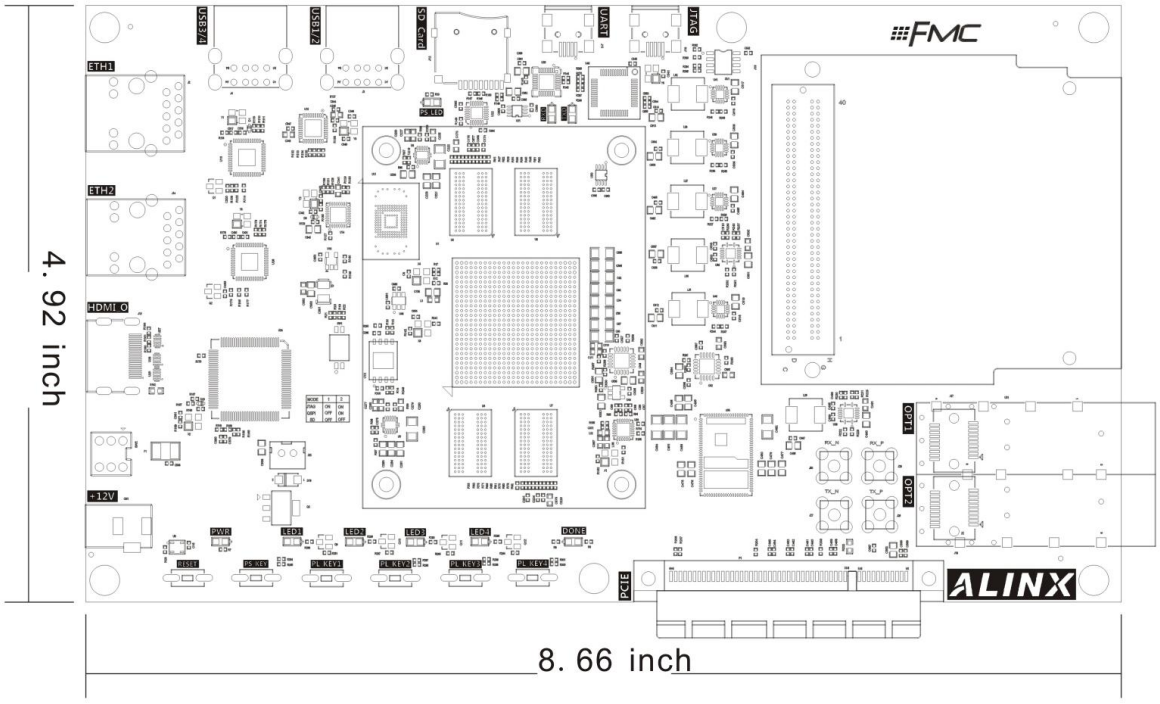


Figure 21-1: Top View