ARTIX-7 FPGA Development Board AX7202

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.2	2023-02-23	Rachel Zhou	First Release

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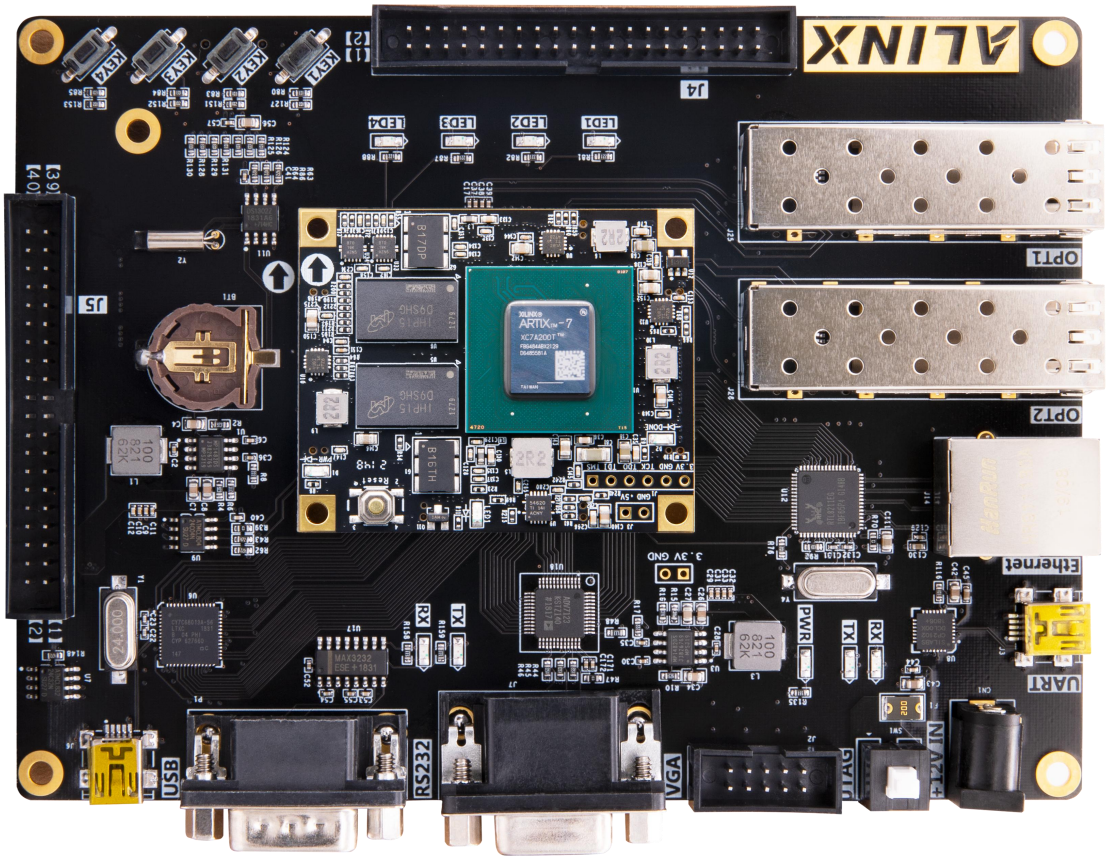
This ARTIX-7 FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development.

In the design of carrier board, we have extended a wealth of interfaces for users, such as 2 fiber interfaces, 1 Gigabit Ethernet interfaces, 1 USB2.0 , VGT output interface, RS232 interface etc. It meets user's requirements for high-speed data exchange, video transmission processing and industrial control. It is a "Versatile" ARTIX-7 FPGA development platform. It provides the possibility for high-speed video transmission, pre-validation and post-application of network and fiber communication and data processing. This product is very suitable for students, engineers and other groups engaged in ARTIX-7FPGA development.



Part 1: FPGA Development Board Introduction

The entire structure of the AX7202 FPGA development board is inherited from our consistent core board + carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of FPGA + 2 DDR3 + QSPI FLASH, which undertakes the functions of high-speed data processing and storage of FPGA, high-speed data reading and writing between FPGA and two DDR3s, data bit width is 32 bits, and the bandwidth of the whole system is up to 25Gb. /s(800M*32bit); The two DDR3 capacities are up to 8Gbit, which meets the need for high buffers during data processing. The selected FPGA is the XC7A200T chip of XILINX's ARTIX-7 series, in BGA 484 package. The communication frequency between the XC7A200T and DDR3 reaches 400Mhz and the data rate is 800Mhz, which fully meets the needs of high-speed multi-channel data processing. In addition, the XC7A200T FPGA features four GTP high-speed transceivers with speeds up to 6.6Gb/s per channel, making it ideal for fiber-optic communications and PCIe data communications.

The AX7202 carrier board expands its rich peripheral interface, including 2 SFP interfaces, 1 Gigabit Ethernet interfaces, 1 USB2.0 HOST interfaces, 1 VGA output interface, 1 RS232 interface, 1 UART serial interface. 1 SD card interface, 2-way 40-pin expansion header, some keys and RTC circuit.

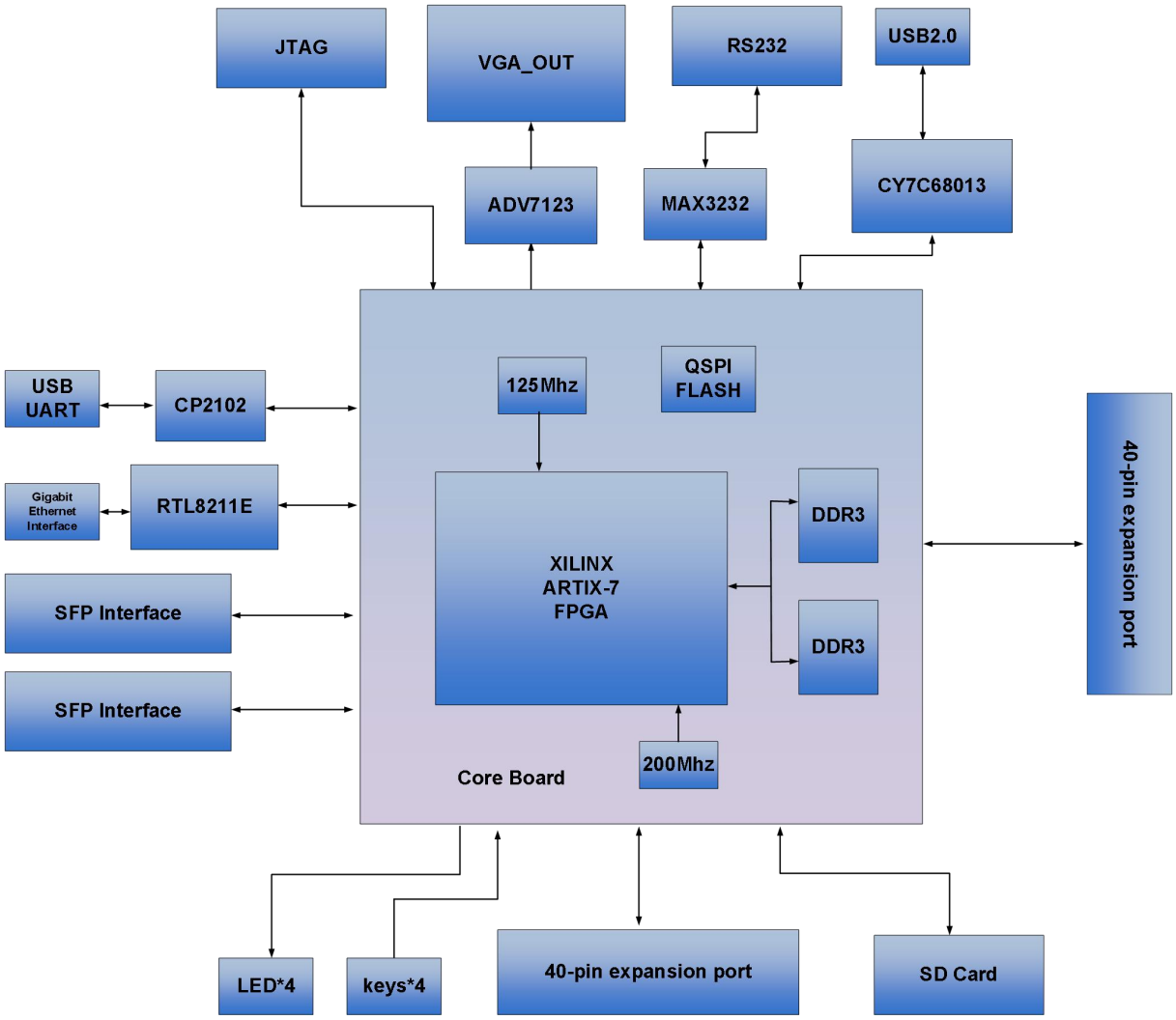


Figure 1-1-1: The Schematic Diagram of the AX7202

Through this diagram, you can see the interfaces and functions that the AX7202 FPGA Development Board contains:

- Artix-7 FPGA core board

  The core board consists of XC7A200T + 8Gb DDR3 + 128Mb QSPI FLASH. There are two high-precision Sitime LVDS differential crystals, one at 200MHz and the other at 148.5MHz, providing stable clock input for FPGA systems and GTP modules.

- 1-channel Gigabit Ethernet Interface RJ-45 interface

  The Gigabit Ethernet interface chip uses Realtek's RTL8211EG Ethernet PHY chip to provide network communication services to users.

RTL8211EG chip supports 10/100/1000 Mbps network transmission rate. Full duplex and adaptive

- 2-channel high-speed SFP Interface

  The two high-speed transceivers of the GTP transceiver of ARTIX-7 FPGA are connected to the transmission and reception of two optical modules to realize two high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds up to 6.6 Gb/s.

- 1-channel VGA Output interface

  The development board uses ADI's ADV7123 chip to achieve VGA output, realizing 24-bit true color RGB digital signal analog conversion, resolution up to 1080p@60Hz output.

- 1-channel USB2.0 Interface

  USB2.0 high-speed communication between FPGA development board and PC is realized by Cypress CY7C68013A USB2.0 controller chip;

- 1-channel Uart to USB interface

  1 Uart to USB interface for communication with the computer for user debugging. The serial port chip is the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface is the MINI USB interface.

- 1-channel RS232 interface

  Uart to RS232 interface for data communication with a computer or other settings. The RS232 conversion chip is the MAX323, and the RS232 interface uses the standard DB9 interface.

- Micro SD card slot

  1-port Micro SD card holder, support SD mode and SPI mode

- RTC real time clock

  Onboard RTC real time clock with battery holder, battery model CR1220

- EEPROM

Onboard an IIC interface EEPROM 24LC04

- 2-way 40-pin expansion port

  2-way 40-pin 0.1inch spacing expansion port can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1 channel 5V power supply, 2 channel 3.3V power supply, 3 way ground, 34 IOs port.

- JTAG Interface

  A 10-pin 0.1 spacing standard JTAG ports for FPGA program download and debugging.

- keys

  4 keys; 1 reset key (on the core board)

- LED Light

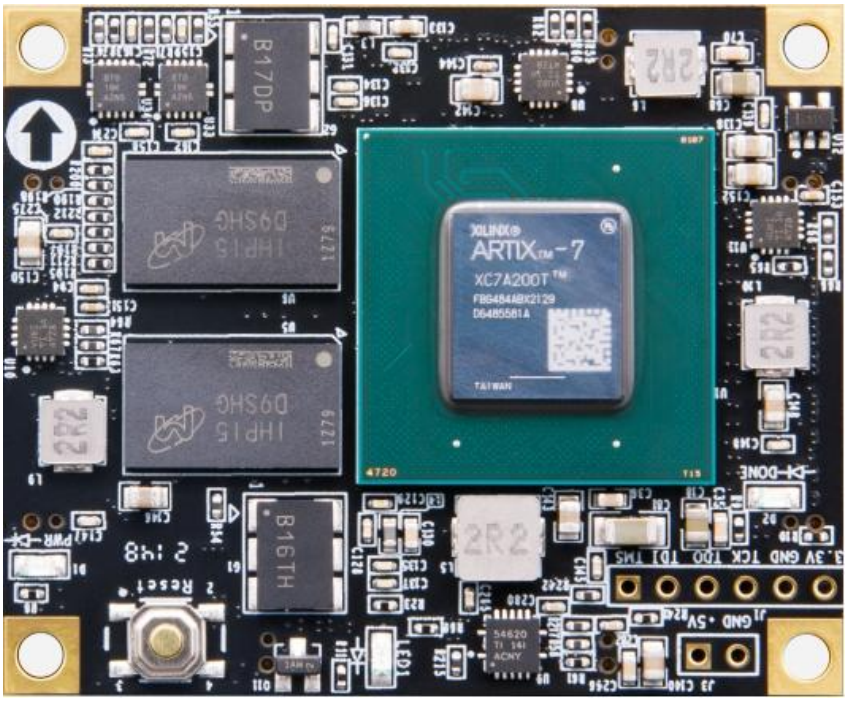
  5 user LEDs (1 on the core board and 4 on the carrier board)

Part 2: AC7200 Core Board Introduction

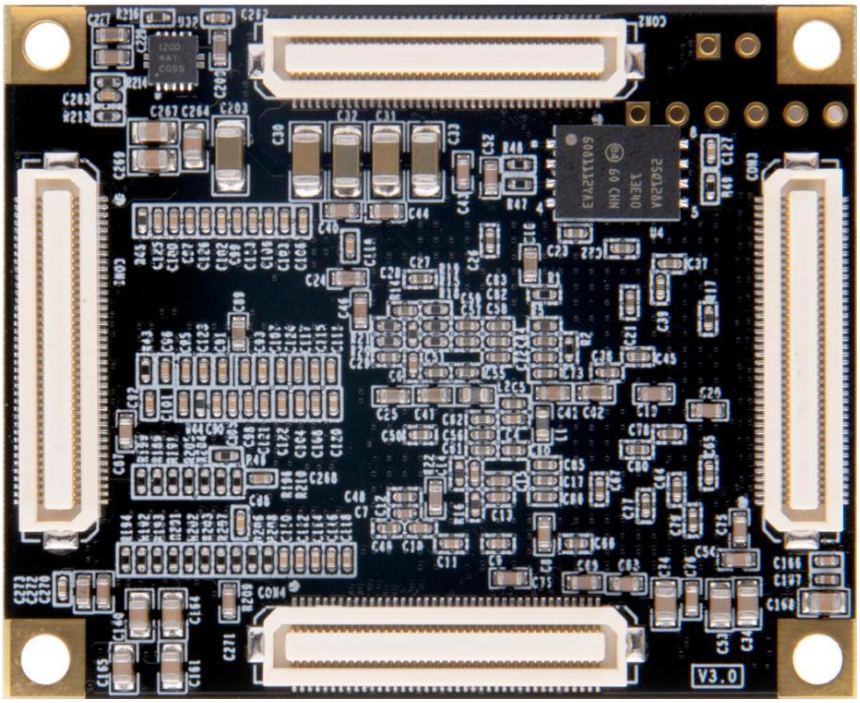
AC7200 (core board model, the same below) FPGA core board, it is based on XILINX's ARTIX-7 series 200T AC7200-2FGG484I. It is a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for high-speed data communication, video image processing, high-speed data acquisition, etc.

This AC7200 core board uses two pieces of MICRON's MT41J256M16HA-125 DDR3 chip, each DDR has a capacity of 4Gbit; two DDR chips are combined into a 32-bit data bus width, and the read/write data bandwidth between FPGA and DDR3 is up to 25Gb; such a configuration can meet the needs of high bandwidth data processing.

The AC7200 core board expands 180 standard IO ports of 3.3V level, 15 standard IO ports of 1.5V level, and 4 pairs of GTP high speed RX/TX differential signals. For users who need a lot of IO, this core board will be a good choice. Moreover, the routing between the FPGA chip and the interface is equal length and differential processing, and the core board size is only 45*55 (mm), which is very suitable for secondary development.



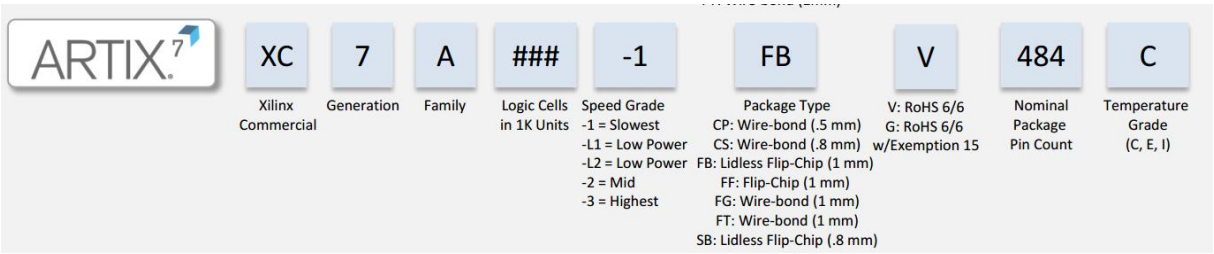
AC7200 Core Board (Front View)



AC7200 Core Board (Rear View)

Part 2.1: FPGA Chip

As mentioned above, the FPGA model we use is AC7200-2FGG484I, which belongs to Xilinx's Artix-7 series. The speed grade is 2, and the temperature grade is industry grade. This model is a FGG484 package with 484 pins. Xilinx ARTIX-7 FPGA chip naming rules as below



The Specific Chip Model Definition of ARTIX-7 Series

FPGA chip on board

The main parameters of the FPGA chip AC7200 are as follows

Name	Specific parameters
Logic Cells	215360
Slices	33650
CLB flip-flops	269200
Block RAM （kb）	13140
DSP Slices	740

PCIe Gen2	1
XADC	1 XADC,12bit, 1Mbps AD
GTP Transceiver	4 GTP，6.6Gb/s max
Speed Grade	-2
Temperature Grade	Industrial

FPGA power supply system

Artix-7 FPGA power supplies are V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the FPGA core power supply pin, which needs to be connected to 1.0V; V_{CCBRAM} is the power supply pin of FPGA block RAM, connect to 1.0V; V_{CCAUX} is FPGA auxiliary power supply pin, connect 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK13~16, BANK34~35. On AC7200 FPGA core board, BANK34 and BANK35 need to be connected to DDR3, the voltage connection of BANK is 1.5V, and the voltage of other BANK is 3.3V. The VCCO of BANK15 and BANK16 is powered by the LDO, and can be changed by replacing the LDO chip. VMGTAVCC is the supply voltage of the FPGA internal GTP transceiver, connected to 1.0V; VMGTAVTT is the termination voltage of the GTP transceiver, connected to 1.2V.

The Artix-7 FPGA system requires that the power-up sequence be powered by VCCINT, then VCCBRAM, then VCCAUX, and finally VCCO. If VCCINT and VCCBRAM have the same voltage, they can be powered up at the same time. The order of power outages is reversed. The power-up sequence of the GTP transceiver is VCCINT, then VMGTAVCC, then VMGTAVTT. If VCCINT and VMGTAVCC have the same voltage, they can be powered up at the same time. The power-off sequence is just the opposite of the power-on sequence.

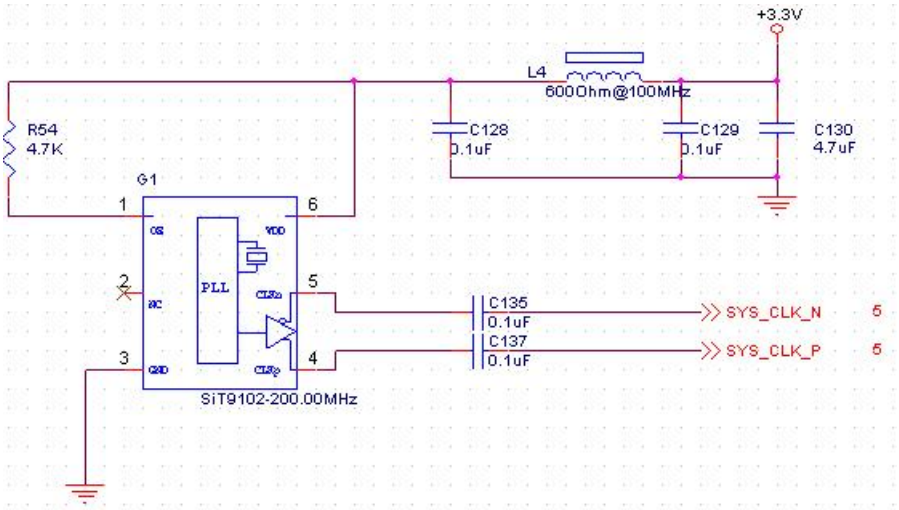
Part 2.2: Active Differential Crystal

The AC7200 core board is equipped with two Sitime active differential crystals, one is 200MHz, the model is SiT9102-200.00MHz, the system main

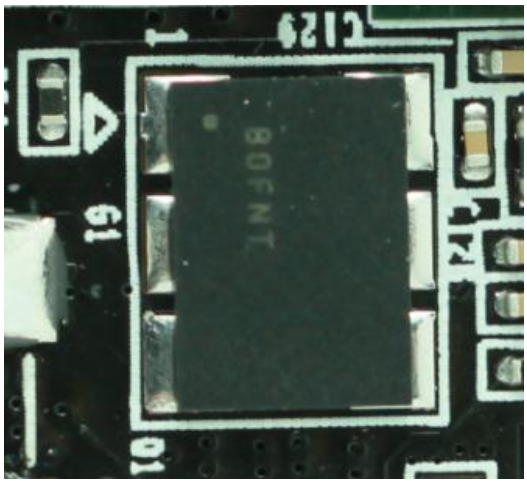
clock for FPGA and used to generate DDR3 control clock; the other is 125MHz, model is SiT9102 -125MHz, reference clock input for GTP transceivers.

Part 2.3: 200Mhz Active Differential clock

G1 in Figure 3-1 is the 200M active differential crystal that provides the development board system clock source. The crystal output is connected to the BANK34 global clock pin MRCC (R4 and T4) of the FPGA. This 200Mhz differential clock can be used to drive the user logic in the FPGA. Users can configure the PLLs and DCMs inside the FPGA to generate clocks of different frequencies.



200Mhz Active Differential Crystal Schematic



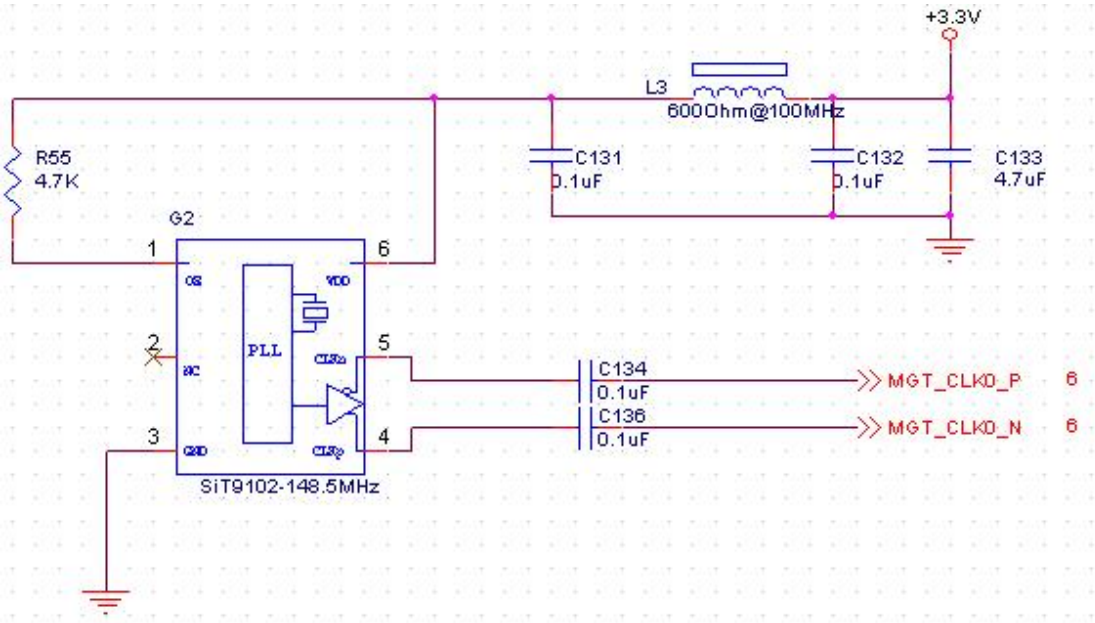
200Mhz Active Differential Crystal on the Core Board

200Mhz Differential Clock Pin Assignment

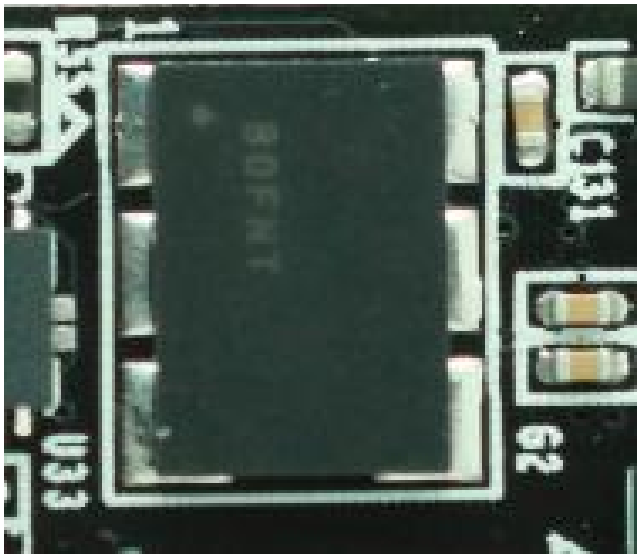
Signal Name	FPGA PIN
SYS_CLK_P	R4
SYS_CLK_N	T4

Part 2.4: 148.5Mhz Active Differential Crystal

G2 is the 148.5Mhz active differential crystal, which is the reference input clock provided to the GTP module inside the FPGA. The crystal output is connected to the GTP BANK216 clock pins MGTREFCLK0P (F6) and MGTREFCLK0N (E6) of the FPGA.



148.5Mhz Active Differential Crystal Schematic



1148.5Mhz Active Differential Crystal on the Core Board

125Mhz Differential Clock Pin Assignment

Net Name	FPGA PIN
MGT_CLK0_P	F6
MGT_CLK0_N	E6

Part 2.5: DDR3 DRAM

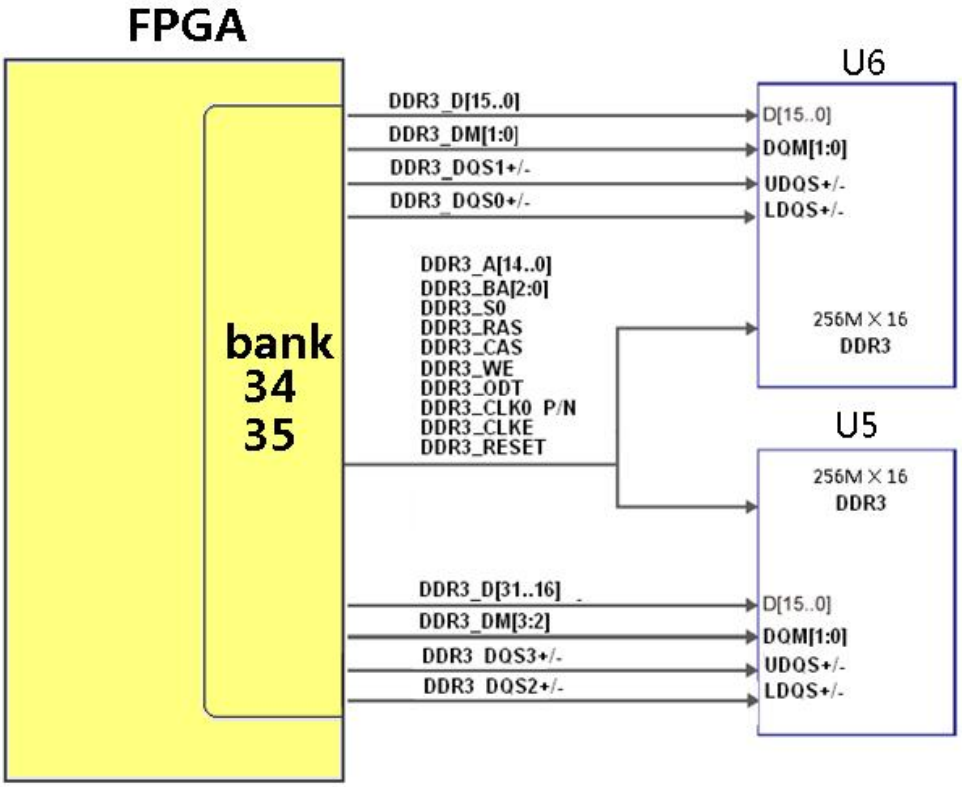
The FPGA core board AC7200 is equipped with two Micron 4Gbit (512MB) DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125). The DDR3 SDRAM has a maximum operating speed of 800MHz (data rate 1600Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 34 and BANK35 of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 4-1.

Bit Number	Chip Model	Capacity	Factory
U5,U6	MT41J256M16HA-125	256M x 16bit	Micron

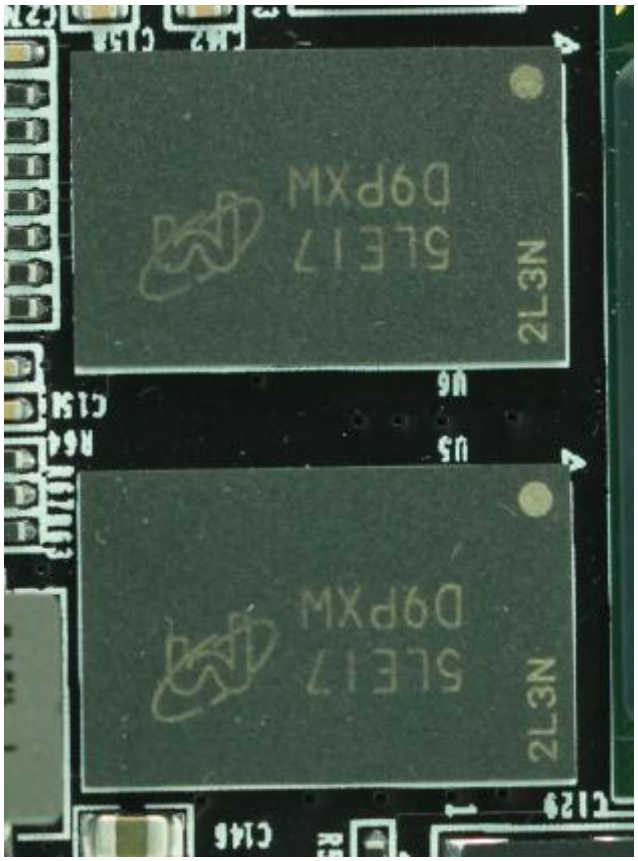
DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance,

trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.



The DDR3 DRAM Schematic



The DDR3 on the Core Board

DDR3 DRAM pin assignment:

Net Name	FPGA PIN Name	FPGA P/N
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1
DDR3_DQ [3]	IO_L6P_T0_35	F3
DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1

DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3
DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5
DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3
DDR3_DQ [21]	IO_L17P_T2_35	K6
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	J4
DDR3_DQ [23]	IO_L18P_T2_35	L5
DDR3_DQ [24]	IO_L20N_T3_35	P1
DDR3_DQ [25]	IO_L19P_T3_35	N4
DDR3_DQ [26]	IO_L20P_T3_35	R1
DDR3_DQ [27]	IO_L22N_T3_35	N2
DDR3_DQ [28]	IO_L23P_T3_35	M6
DDR3_DQ [29]	IO_L24N_T3_35	N5
DDR3_DQ [30]	IO_L24P_T3_35	P6
DDR3_DQ [31]	IO_L22P_T3_35	P2
DDR3_DM0	IO_L4N_T0_35	D2
DDR3_DM1	IO_L8N_T1_AD14N_35	G2
DDR3_DM2	IO_L16N_T2_35	M2
DDR3_DM3	IO_L23N_T3_35	M5
DDR3_A[0]	IO_L11N_T1_SRCC_34	AA4
DDR3_A[1]	IO_L8N_T1_34	AB2
DDR3_A[2]	IO_L10P_T1_34	AA5
DDR3_A[3]	IO_L10N_T1_34	AB5
DDR3_A[4]	IO_L7N_T1_34	AB1
DDR3_A[5]	IO_L6P_T0_34	U3

DDR3_A[6]	IO_L5P_T0_34	W1
DDR3_A[7]	IO_L1P_T0_34	T1
DDR3_A[8]	IO_L2N_T0_34	V2
DDR3_A[9]	IO_L2P_T0_34	U2
DDR3_A[10]	IO_L5N_T0_34	Y1
DDR3_A[11]	IO_L4P_T0_34	W2
DDR3_A[12]	IO_L4N_T0_34	Y2
DDR3_A[13]	IO_L1N_T0_34	U1
DDR3_A[14]	IO_L6N_T0_VREF_34	V3
DDR3_BA[0]	IO_L9N_T1_DQS_34	AA3
DDR3_BA[1]	IO_L9P_T1_DQS_34	Y3
DDR3_BA[2]	IO_L11P_T1_SRCC_34	Y4
DDR3_S0	IO_L8P_T1_34	AB3
DDR3_RAS	IO_L12P_T1_MRCC_34	V4
DDR3_CAS	IO_L12N_T1_MRCC_34	W4
DDR3_WE	IO_L7P_T1_34	AA1
DDR3_ODT	IO_L14N_T2_SRCC_34	U5
DDR3_RESET	IO_L15P_T2_DQS_34	W6
DDR3_CLK_P	IO_L3P_T0_DQS_34	R3
DDR3_CLK_N	IO_L3N_T0_DQS_34	R2
DDR3_CKE	IO_L14P_T2_SRCC_34	T5

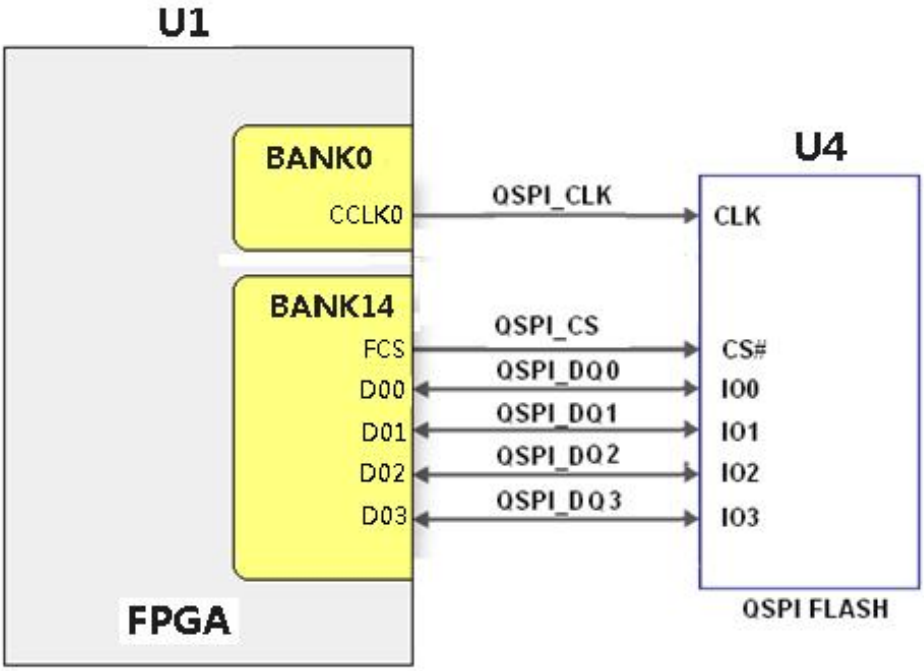
Part 2.6: QSPI Flash

The FPGA core board AC7200 is equipped with one 128MBit QSPI FLASH, and the model is W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, core application code and other user data files. The specific models and related parameters of QSPI FLASH are shown .

Position	Model	Capacity	Factory
U8	N25Q128	128M Bit	Numonyx

QSPI FLASH Specification

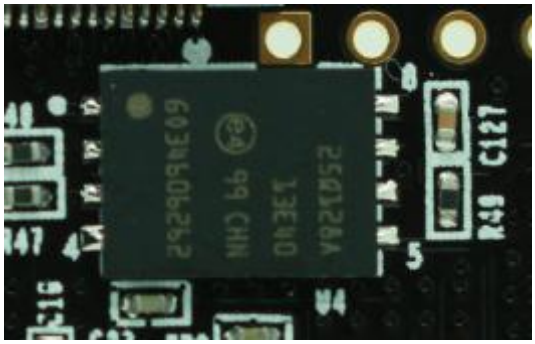
QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip select signals are connected to D00~D03 and FCS pins of BANK14 respectively. Shows the hardware connection of QSPI Flash.



QSPI Flash Schematic

QSPI Flash pin assignments:

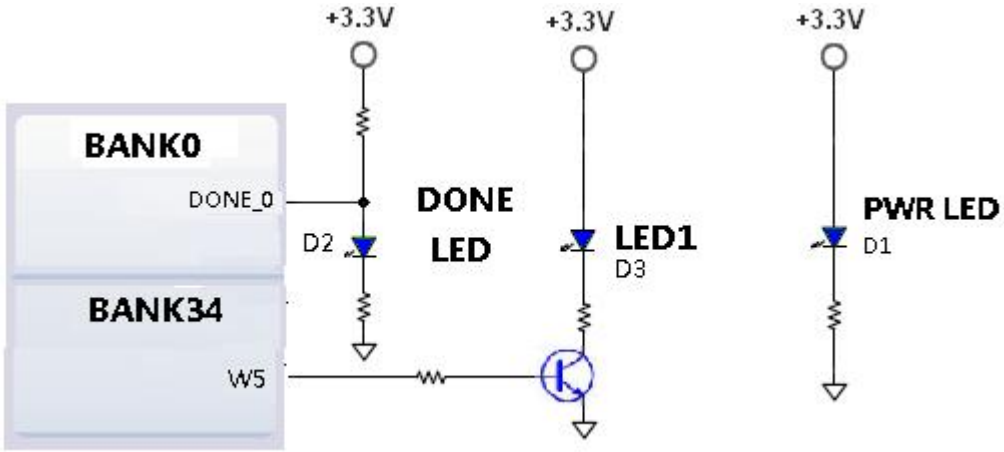
Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21



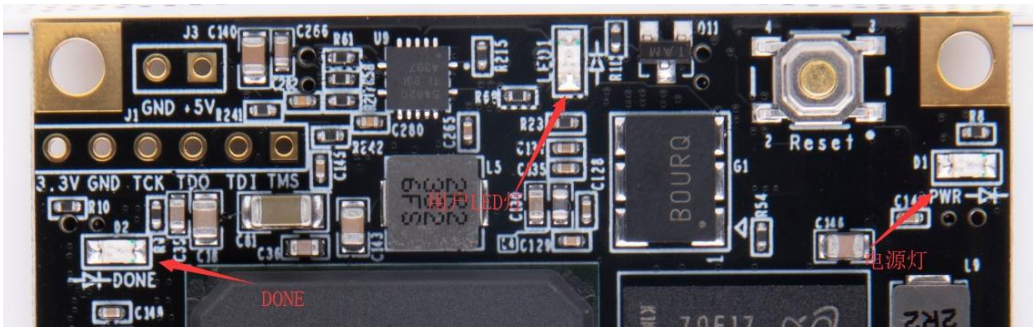
QSPI on the Core Board

Part 2.7: LED Light on Core Board

There are 3 red LED lights on the AC7200 FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. The user LED light is connected to the IO of the BANK34, the user can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED is off. When the connection IO voltage is low, the user LED will be lit. The schematic diagram of the LED light hardware connection is shown:



LED lights on core board Schematic



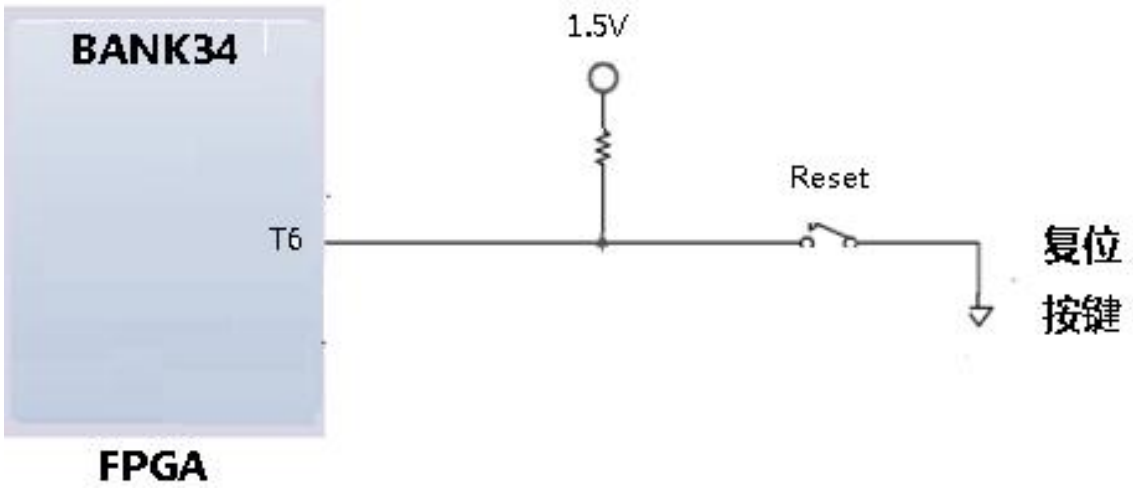
LED lights on the Core Board

User LEDs Pin Assignment

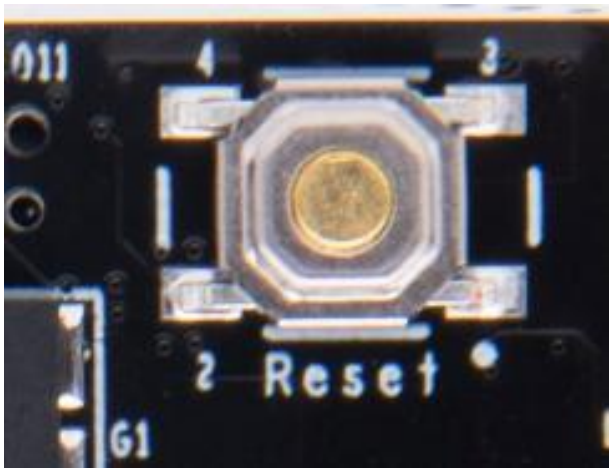
Signal Name	FPGA Pin Name	FPGA Pin Number	Description
LED1	IO_L15N_T2_DQS_34	W5	User LED

Part 2.8: Reset Button

There is a reset button on the AC7200 FPGA core board. The reset button is connected to the normal IO of the BANK34 of the FPGA chip. The user can use this reset button to initialize the FPGA program. When the button is pressed in the design, the signal voltage input to IO is low, and the reset signal is valid; when the button is not pressed, the signal input to IO is high. The schematic diagram of the reset button connection is shown:



Reset Button Schematic



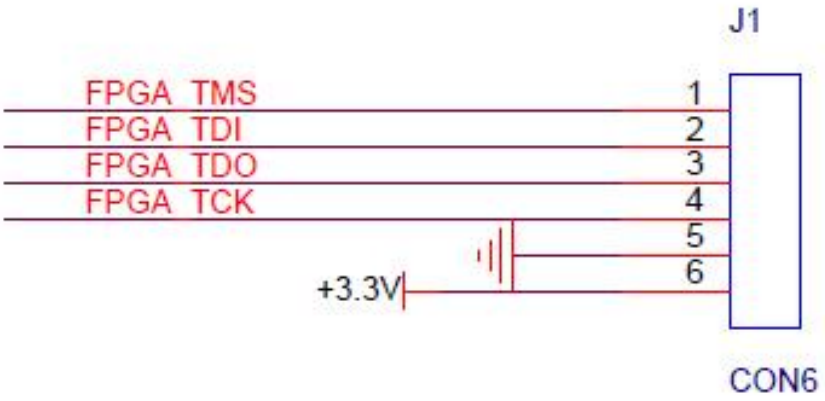
Reset button on the Core Board

Reset button pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
RESET_N	IO_L17N_T2_34	T6	FPGA system reset

Part 2.9: JTAG Interface

The JTAG test socket J1 is reserved on the AC7200 core board for JTAG download and debugging when the core board is used alone. Figure is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK. , GND, +3.3V these six signals.



JTAG Interface Schematic

The JTAG interface J1 on AC7200 FPGA core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connection to debug on the core board, you need to solder a 6-pin single-row pin header. shows the JTAG interface J1 on the AC7200 FPGA core board.

JTAG Interface on Core Board

Part 2.10: Power Interface on the Core Board

In order to make the AC7200 FPGA core board work alone, the core board is reserved with the 2PIN power interface (J3). When the user supplies power to the core board through 2PIN power interface (J3), it cannot be powered through the carrier board. Otherwise, current conflict may occur.

Power Interface on the Core Board

Part 2.11: Board to Board Connectors

The core board has a total of four high-speed board to board connectors. The core board uses four 80-pin inter-board connectors to connect to the carrier board. The IO port of the FPGA is connected to the four connectors by differential routing. The pin spacing of the connectors is 0.5mm, insert to the board to board connectors on the carrier board for high-speed data communication.

The core board has a total of four high-speed board to board connectors. The core board uses four 80-pin inter-board connectors to connect to the carrier board. The IO port of the FPGA is connected to the four connectors by differential routing. The pin spacing of the connectors is 0.5mm, insert to the board to board connectors on the carrier board for high-speed data communication.

Board to Board Connectors CON1

The 80-pin board to board connectors CON1, which are used to connect with the VCCIN power supply (+5V) and ground on the carrier board, extend the normal IOs of the FPGA. It should be noted here that 15 pins of CON1 are connected to the IO port of BANK34, because the BANK34 connection is connected to DDR3. Therefore, the voltage standard of all IOs of this BANK34 is 1.5V.

Pin Assignment of Board to Board Connectors CON1

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	VCCIN	-	+5V	PIN2	VCCIN	-	+5V
PIN3	VCCIN	-	+5V	PIN4	VCCIN	-	+5V
PIN5	VCCIN	-	+5V	PIN6	VCCIN	-	+5V
PIN7	VCCIN	-	+5V	PIN8	VCCIN	-	+5V
PIN9	GND	-	Ground	PIN10	GND	-	Ground

PIN11	NC	-	-	PIN12	NC	-	-
PIN13	NC	-	-	PIN14	NC	-	-
PIN15	NC	-	-	PIN16	B13_L4_P	AA15	3.3V
PIN17	NC	-	-	PIN18	B13_L4_N	AB15	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L5_P	Y13	3.3V	PIN22	B13_L1_P	Y16	3.3V
PIN23	B13_L5_N	AA14	3.3V	PIN24	B13_L1_N	AA16	3.3V
PIN25	B13_L7_P	AB11	3.3V	PIN26	B13_L2_P	AB16	3.3V
PIN27	B13_L7_P	AB12	3.3V	PIN28	B13_L2_N	AB17	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L3_P	AA13	3.3V	PIN32	B13_L6_P	W14	3.3V
PIN33	B13_L3_N	AB13	3.3V	PIN34	B13_L6_N	Y14	3.3V
PIN35	B34_L23_P	Y8	1.5V	PIN36	B34_L20_P	AB7	1.5V
PIN37	B34_L23_N	Y7	1.5V	PIN38	B34_L20_N	AB6	1.5V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B34_L18_N	AA6	1.5V	PIN42	B34_L21_N	V8	1.5V
PIN43	B34_L18_P	Y6	1.5V	PIN44	B34_L21_P	V9	1.5V
PIN45	B34_L19_P	V7	1.5V	PIN46	B34_L22_P	AA8	1.5V
PIN47	B34_L19_N	W7	1.5V	PIN48	B34_L22_N	AB8	1.5V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	XADC_VN	M9	ADC	PIN52	NC		
PIN53	XADC_VP	L10	ADC	PIN54	B34_L25	U7	1.5V
PIN55	NC	-	-	PIN56	B34_L24_P	W9	1.5V
PIN57	NC	-	-	PIN58	B34_L24_N	Y9	1.5V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L1_N	F14	3.3V	PIN62	NC	-	-
PIN63	B16_L1_P	F13	3.3V	PIN64	NC	-	-
PIN65	B16_L4_N	E14	3.3V	PIN66	NC	-	-
PIN67	B16_L4_P	E13	3.3V	PIN68	NC	-	-
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L6_N	D15	3.3V	PIN72	NC	-	-

Board to Board Connectors CON2

The 80-pin female connection header CON2 is used to extend the normal IO of the BANK13 and BANK14 of the FPGA. The voltage standards of both BANKs are 3.3V.

Pin Assignment of Board to Board Connectors CON2

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	B13_L16_P	W15	3.3V	PIN2	B14_L16_P	V17	3.3V
PIN3	B13_L16_N	W16	3.3V	PIN4	B14_L16_N	W17	3.3V
PIN5	B13_L15_P	T14	3.3V	PIN6	B13_L14_P	U15	3.3V
PIN7	B13_L15_N	T15	3.3V	PIN8	B13_L14_N	V15	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B13_L13_P	V13	3.3V	PIN12	B14_L10_P	AB21	3.3V
PIN13	B13_L13_N	V14	3.3V	PIN14	B14_L10_N	AB22	3.3V
PIN15	B13_L12_P	W11	3.3V	PIN16	B14_L8_N	AA21	3.3V
PIN17	B13_L12_N	W12	3.3V	PIN18	B14_L8_P	AA20	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L11_P	Y11	3.3V	PIN22	B14_L15_N	AB20	3.3V
PIN23	B13_L11_N	Y12	3.3V	PIN24	B14_L15_P	AA19	3.3V
PIN25	B13_L10_P	V10	3.3V	PIN26	B14_L17_P	AA18	3.3V
PIN27	B13_L10_N	W10	3.3V	PIN28	B14_L17_N	AB18	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L9_N	AA11	3.3V	PIN32	B14_L6_N	T20	3.3V
PIN33	B13_L9_P	AA10	3.3V	PIN34	B13_IO0	Y17	3.3V
PIN35	B13_L8_N	AB10	3.3V	PIN36	B14_L7_N	W22	3.3V
PIN37	B13_L8_P	AA9	3.3V	PIN38	B14_L7_P	W21	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B14_L11_N	V20	3.3V	PIN42	B14_L4_P	T21	3.3V
PIN43	B14_L11_P	U20	3.3V	PIN44	B14_L4_N	U21	3.3V
PIN45	B14_L14_N	V19	3.3V	PIN46	B14_L9_P	Y21	3.3V
PIN47	B14_L14_P	V18	3.3V	PIN48	B14_L9_N	Y22	3.3V

PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B14_L5_N	R19	3.3V	PIN52	B14_L12_N	W20	3.3V
PIN53	B14_L5_P	P19	3.3V	PIN54	B14_L12_P	W19	3.3V
PIN55	B14_L18_N	U18	3.3V	PIN56	B14_L13_N	Y19	3.3V
PIN57	B14_L18_P	U17	3.3V	PIN58	B14_L13_P	Y18	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B13_L17_P	T16	3.3V	PIN62	B14_L3_N	V22	3.3V
PIN63	B13_L17_N	U16	3.3V	PIN64	B14_L3_P	U22	3.3V
PIN65	B14_L21_N	P17	3.3V	PIN66	B14_L20_N	T18	3.3V
PIN67	B14_L21_P	N17	3.3V	PIN68	B14_L20_P	R18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B14_L22_P	P15	3.3V	PIN72	B14_L19_N	R14	3.3V
PIN73	B14_L22_N	R16	3.3V	PIN74	B14_L19_P	P14	3.3V
PIN75	B14_L24_N	R17	3.3V	PIN76	B14_L23_P	N13	3.3V
PIN77	B14_L24_P	P16	3.3V	PIN78	B14_L23_N	N14	3.3V
PIN79	B14_IO0	P20	3.3V	PIN80	B14_IO25	N15	3.3V

Board to Board Connectors CON3

The 80-pin connector CON3 is used to extend the normal IO of the BANK15 and BANK16 of the FPGA. In addition, four JTAG signals are also connected to the carrier board via the CON3 connector. The voltage standards of BANK15 and BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V. If you want to output other standard levels, you can replace it with a suitable LDO.

Pin Assignment of Board to Board Connectors CON3

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	B15_IO0	J16	3.3V	PIN2	B15_IO25	M17	3.3V
PIN3	B16_IO0	F15	3.3V	PIN4	B16_IO25	F21	3.3V
PIN5	B15_L4_P	G17	3.3V	PIN6	B16_L21_N	A21	3.3V
PIN7	B15_L4_N	G18	3.3V	PIN8	B16_L21_P	B21	3.3V

PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B15_L2_P	G15	3.3V	PIN12	B16_L23_P	E21	3.3V
PIN13	B15_L2_N	G16	3.3V	PIN14	B16_L23_N	D21	3.3V
PIN15	B15_L12_P	J19	3.3V	PIN16	B16_L22_P	E22	3.3V
PIN17	B15_L12_N	H19	3.3V	PIN18	B16_L22_N	D22	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B15_L11_P	J20	3.3V	PIN22	B16_L24_P	G21	3.3V
PIN23	B15_L11_N	J21	3.3V	PIN24	B16_L24_N	G22	3.3V
PIN25	B15_L1_N	G13	3.3V	PIN26	B15_L8_N	G20	3.3V
PIN27	B15_L1_P	H13	3.3V	PIN28	B15_L8_P	H20	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B15_L5_P	J15	3.3V	PIN32	B15_L7_N	H22	3.3V
PIN33	B15_L5_N	H15	3.3V	PIN34	B15_L7_P	J22	3.3V
PIN35	B15_L3_N	H14	3.3V	PIN36	B15_L9_P	K21	3.3V
PIN37	B15_L3_P	J14	3.3V	PIN38	B15_L9_N	K22	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B15_L19_P	K13	3.3V	PIN42	B15_L15_N	M22	3.3V
PIN43	B15_L19_N	K14	3.3V	PIN44	B15_L15_P	N22	3.3V
PIN45	B15_L20_P	M13	3.3V	PIN46	B15_L6_N	H18	3.3V
PIN47	B15_L20_N	L13	3.3V	PIN48	B15_L6_P	H17	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B15_L14_P	L19	3.3V	PIN52	B15_L13_N	K19	3.3V
PIN53	B15_L14_N	L20	3.3V	PIN54	B15_L13_P	K18	3.3V
PIN55	B15_L21_P	K17	3.3V	PIN56	B15_L10_P	M21	3.3V
PIN57	B15_L21_N	J17	3.3V	PIN58	B15_L10_N	L21	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B15_L23_P	L16	3.3V	PIN62	B15_L18_P	N20	3.3V
PIN63	B15_L23_N	K16	3.3V	PIN64	B15_L18_N	M20	3.3V
PIN65	B15_L22_P	L14	3.3V	PIN66	B15_L17_N	N19	3.3V
PIN67	B15_L22_N	L15	3.3V	PIN68	B15_L17_P	N18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B15_L24_P	M15	3.3V	PIN72	B15_L16_P	M18	3.3V

PIN73	B15_L24_N	M16	3.3V	PIN74	B15_L16_N	L18	3.3V
PIN75	NC	-		PIN76	NC	-	
PIN77	FPGA_TCK	V12	3.3V	PIN78	FPGA_TDI	R13	3.3V
PIN79	FPGA_TDO	U13	3.3V	PIN80	FPGA_TMS	T13	3.3V

Board to Board Connectors CON4

The 80-Pin connector CON4 is used to extend the normal IO and GTP high-speed data and clock signals of the FPGA BANK16. The voltage standard of the IO port of BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V. If the user wants to output other standard levels, it can be replaced by a suitable LDO. The high-speed data and clock signals of the GTP are strictly differential routed on the core board. The data lines are equal in length and kept at a certain interval to prevent signal interference.

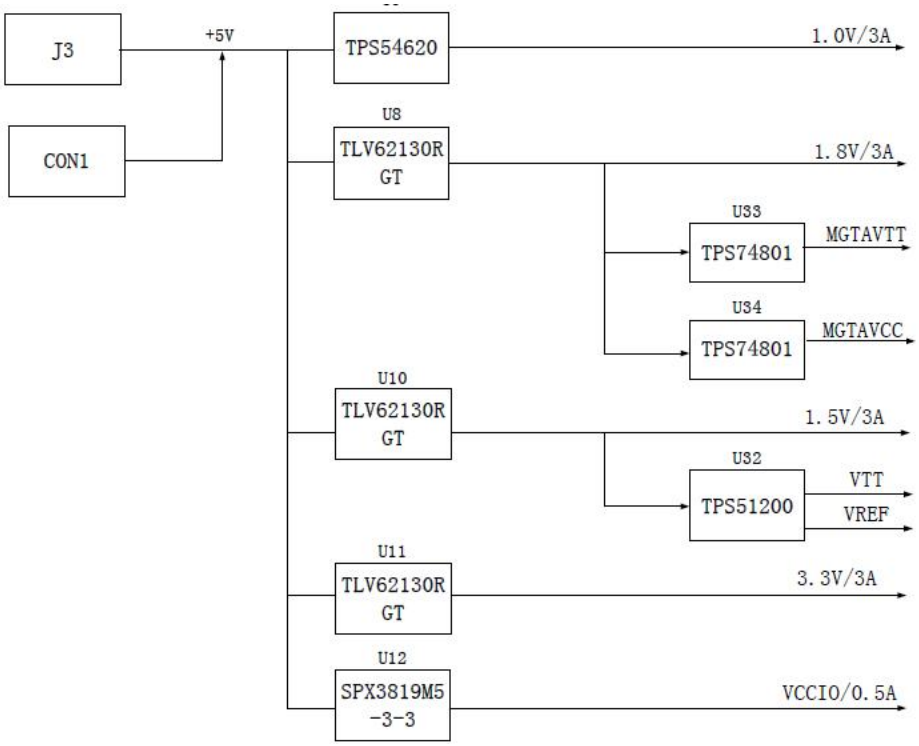
Pin Assignment of Board to Board Connectors CON4

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	NC		-	NC		-	NC
PIN3	NC		-	NC		-	NC
PIN5	NC		-	NC		-	NC
PIN7	NC		-	NC		-	NC
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	NC		-	PIN12	MGT_TX2_P	B6	Differential
PIN13	NC		-	PIN14	MGT_TX2_N	A6	Differential
PIN15	GND	-	Ground	PIN16	GND	-	Ground
PIN17	MGT_TX3_P	D7	Differential	PIN18	MGT_RX2_P	B10	Differential
PIN19	MGT_TX3_N	C7	Differential	PIN20	MGT_RX2_N	A10	Differential
PIN21	GND	-	Ground	PIN22	GND	-	Ground
PIN23	MGT_RX3_P	D9	Differential	PIN24	MGT_TX0_P	B4	Differential
PIN25	MGT_RX3_N	C9	Differential	PIN26	MGT_TX0_N	A4	Differential
PIN27	GND	-	Ground	PIN28	GND	-	Ground
PIN29	MGT_TX1_P	D5	Differential	PIN30	MGT_RX0_P	B8	Differential

PIN31	MGT_TX1_N	C5	Differential	PIN32	MGT_RX0_N	A8	Differential
PIN33	GND	-	Ground	PIN34	GND	-	Ground
PIN35	MGT_RX1_P	D11	Differential	PIN36	MGT_CLK1_P	F10	Differential
PIN37	MGT_RX1_N	C11	Differential	PIN38	MGT_CLK1_N	E10	Differential
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B16_L5_P	E16	3.3V	PIN42	B16_L2_P	F16	3.3V
PIN43	B16_L5_N	D16	3.3V	PIN44	B16_L2_N	E17	3.3V
PIN45	B16_L7_P	B15	3.3V	PIN46	B16_L3_P	C14	3.3V
PIN47	B16_L7_N	B16	3.3V	PIN48	B16_L3_N	C15	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B16_L9_P	A15	3.3V	PIN52	B16_L10_P	A13	3.3V
PIN53	B16_L9_N	A16	3.3V	PIN54	B16_L10_N	A14	3.3V
PIN55	B16_L11_P	B17	3.3V	PIN56	B16_L12_P	D17	3.3V
PIN57	B16_L11_N	B18	3.3V	PIN58	B16_L12_N	C17	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L13_P	C18	3.3V	PIN62	B16_L14_P	E19	3.3V
PIN63	B16_L13_N	C19	3.3V	PIN64	B16_L14_N	D19	3.3V
PIN65	B16_L15_P	F18	3.3V	PIN66	B16_L16_P	B20	3.3V
PIN67	B16_L15_N	E18	3.3V	PIN68	B16_L16_N	A20	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L17_P	A18	3.3V	PIN72	B16_L18_P	F19	3.3V
PIN73	B16_L17_N	A19	3.3V	PIN74	B16_L18_N	F20	3.3V
PIN75	B16_L19_P	D20	3.3V	PIN76	B16_L20_P	C22	3.3V
PIN77	B16_L19_N	C20	3.3V	PIN78	B16_L20_N	B22	3.3V
PIN79	NC	-		PIN80	NC	-	

Part 2.12: Power Supply

The AC7200 FPGA core board is powered by DC5V via carrier board, and it is powered by the J3 interface when it is used alone. Please be careful not to supply power by the J3 interface and the carrier board at the same time to avoid damage. The power supply design diagram on the board is shown in.



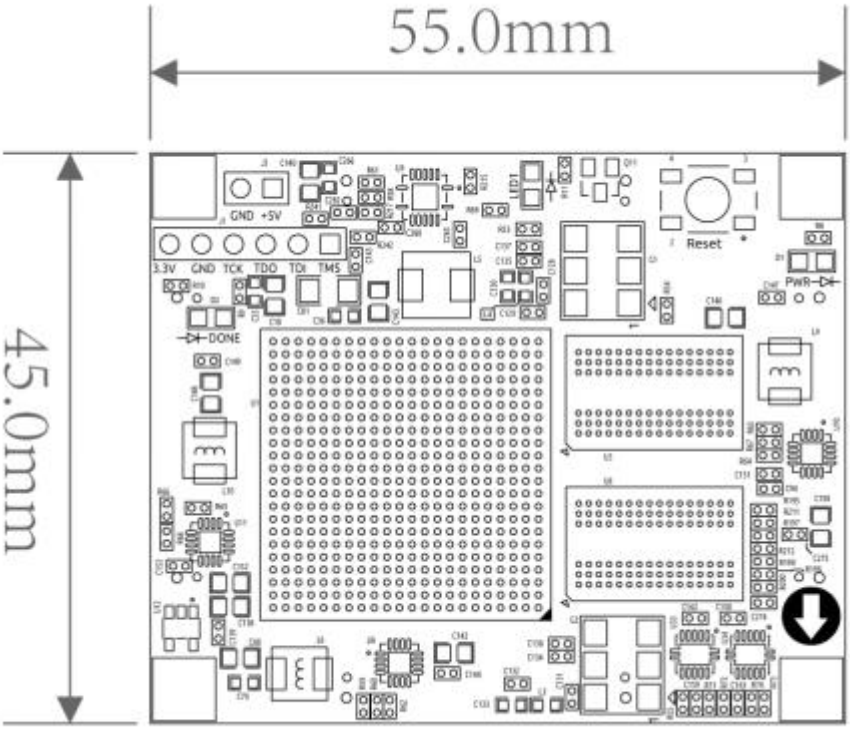
Power Supply on core board schematic

The development board is powered by +5V and converted to +3.3V, +1.5V, +1.8V, +1.0V four-way power supply through four DC/DC power supply chip TLV62130RGT. The output current can be up to 3A per channel. VCCIO is generated by one LDOSPX3819M5-3-3. VCCIO mainly supplies power to BANK15 and BANK16 of FPGA. Users can change the IO of BANK15,16 to different voltage standards by replacing their LDO chip. 1.5V Generates the VTT and VREF voltages required by DDR3 via TI's TPS51200. The 1.8V power supply MGTAVTT MGTAVCC for the GTP transceiver is generated by TI's TPS74801 chip. The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	FPGA Core Voltage
+1.8V	FPGA auxiliary voltage, TPS74801 power supply
+3.3V	VCCIO of Bank0,Bank13 and Bank14 of FPGA,QSIP FLASH, Clock Crystal
+1.5V	DDR3, Bank34 and Bank35 of FPGA
VREF,VTT(+0.75V)	DDR3
MVCCIP(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	GTP Transceiver Bank216 of FPGA
MGTVCCAUX(+1.8V)	GTP Transceiver Bank216 of FPGA

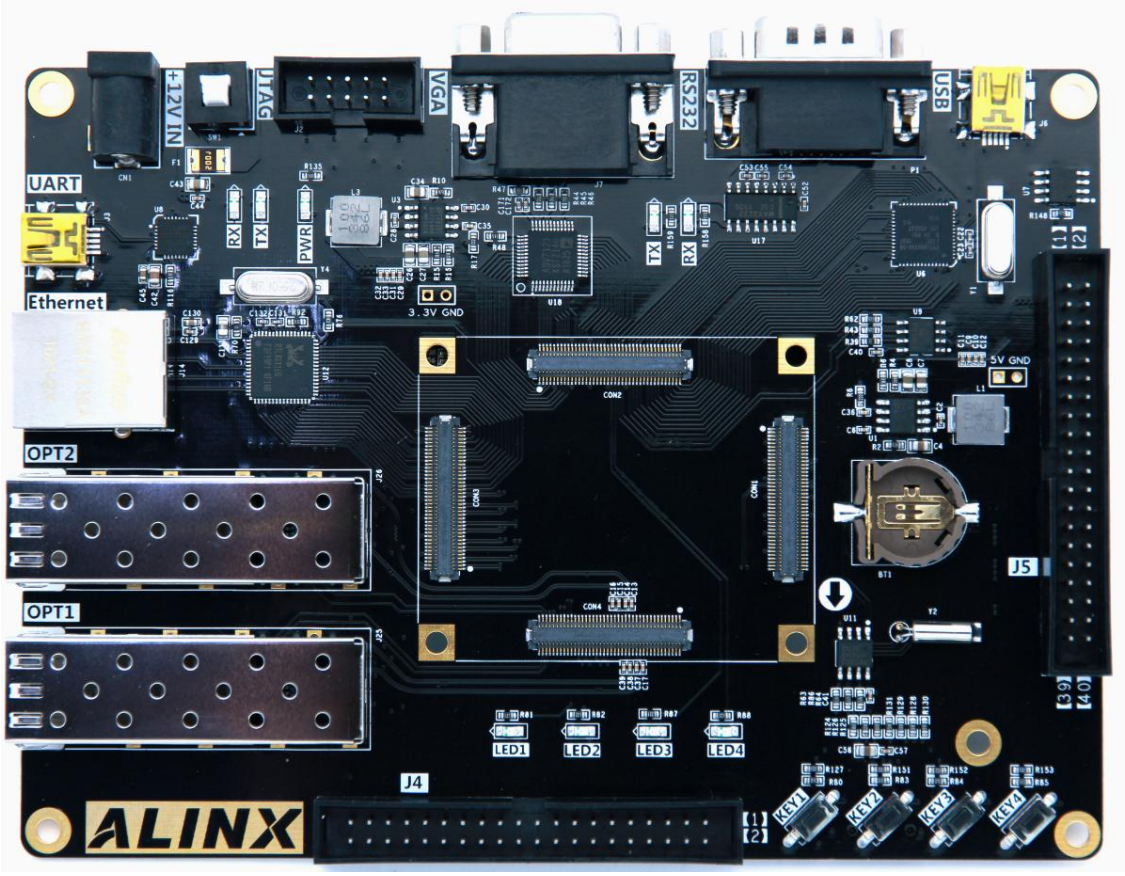
Because the power supply of Artix-7 FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is 1.0V->1.8V->(1.5 V, 3.3V, VCCIO) and 1.0V-> MGTAVCC -> MGTAVTT, the circuit design to ensure the normal operation of the chip.

Part 2.13: Structure Diagram



AC7200 FPGA Core board (Top view)

Part 3: Carrier Board



Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- 1-channel 10/100M/1000M Ethernet RJ-45 interface
- 2-channel SFP interface
- 1-channel 24-bit VGA output interface
- 1-channel USB 2.0 communication interface
- 1-channel USB HOST interface
- 1-channel RS232 communication interface
- 1 SD card slot

- RTC Circuit
- EEPROM
- 2-channel 40-pin expansion ports
- JTAG debugging interface
- 4 independent keys
- 4 user LED lights

Part 3.2: Gigabit Ethernet Interface

The AX7202 carrier board provides users with one-channel Gigabit network communication service through the Realtek RTL8211EG Ethernet PHY chip. The RTL8211EG chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the GMII interface. RTL8211EG supports MDI/MDX adaptation, various speed adaptations, Master/Slave adaptation, and support for MDIO bus for PHY register management.

The RTL8211EG will detect the level status of some specific IOs to determine their working mode after powered on. Table 3-1-1 describes the default setup information after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	3.3V, 2.5V, 1.5/1.8V voltage selection	3.3V
SELRGV	Auto-negotiation configuration	(10/100/1000M) adaptive
AN[1:0]	RX clock 2ns delay	Delay
RX Delay	TX clock 2ns delay	Delay
TX Delay	RGMII or GMII selection	GMII

Table 3-2-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the GMII bus, the transmission clock is 125Mhz. The receive clock E_RXC is

provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is sampled on the rising edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the GMII bus, the transmission clock is 25Mhz. The receive clock E_RXC is provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is sampled on the rising edge of the clock.

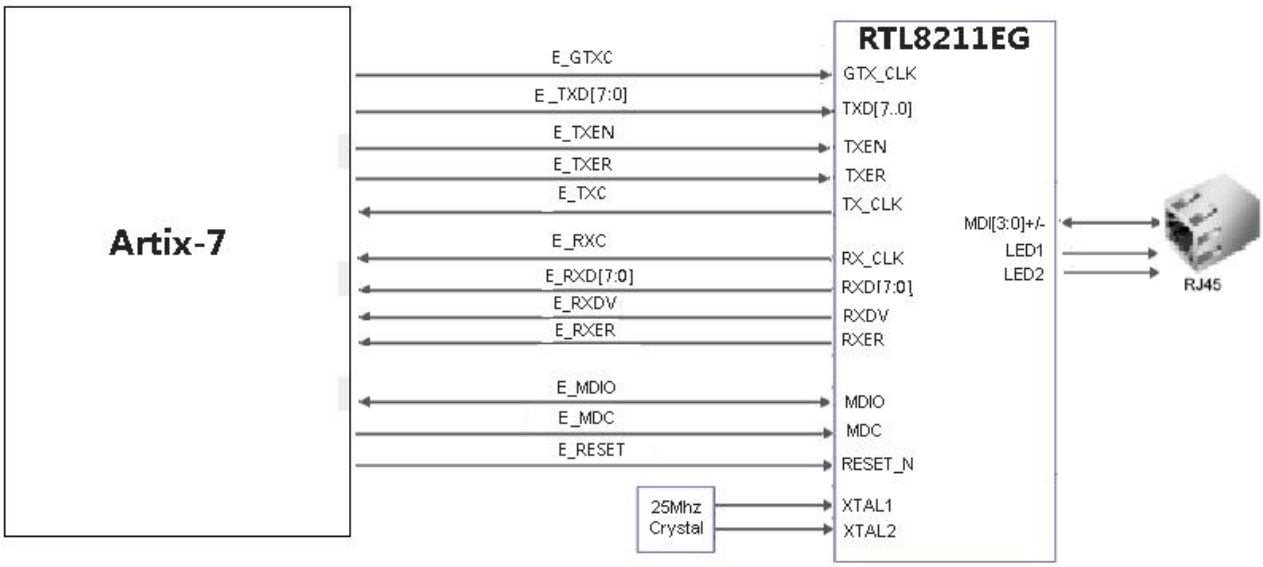


Figure 3-2-1: Gigabit Ethernet Interface Schematic

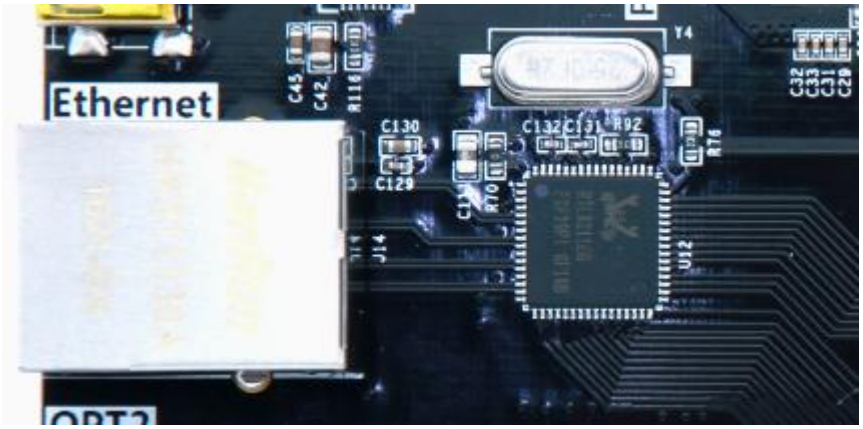


Figure 3-3-2: Gigabit Ethernet interface on the Carrier Board

Gigabit Ethernet pin assignments are as follows：

Signal Name	FPGA PIN	Description

E_GTXC	L18	Ethernet GMII transmit clock
E_TXD0	M15	Ethernet Transmit Data bit0
E_TXD1	L14	Ethernet Transmit Data bit1
E_TXD2	K16	Ethernet Transmit Data bit2
E_TXD3	L16	Ethernet Transmit Data bit3
E_TXD4	K17	Ethernet Transmit Data bit4
E_TXD5	L20	Ethernet Transmit Data bit5
E_TXD6	L19	Ethernet Transmit Data bit6
E_TXD7	L13	Ethernet Transmit Data bit7
E_TXEN	M16	Ethernet transmit enable signal
E_TXER	M13	Ethernet transmit error signal
E_TXC	J17	Ethernet GMII transmit clock
E_RXC	K18	Ethernet GMII receive clock
E_RXDV	M22	Ethernet receive data valid signal
E_RXER	N19	Ethernet receiving data error
E_RXD0	N22	Ethernet Receive Data Bit0
E_RXD1	H18	Ethernet Receive Data Bit1
E_RXD2	H17	Ethernet Receive Data Bit2
E_RXD3	K19	Ethernet Receive Data Bit3
E_RXD4	M21	Ethernet Receive Data Bit4
E_RXD5	L21	Ethernet Receive Data Bit5
E_RXD6	N20	Ethernet Receive Data Bit6
E_RXD7	M20	Ethernet Receive Data Bit7
E_COL	N18	Ethernet Collision signal
E_CRS	M18	Ethernet “Carrier Sense” Signal
E_RESET	L15	Ethernet Reset Signal
E_MDC	W10	Ethernet MDIO Management Clock
E_MDIO	V10	Ethernet MDIO Management Data

Part 3.3: SFP Interface

The AX7202 Carrier board has two optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5G optical modules on the market) and insert them into these two optical interfaces for optical data communication. The two fiber interfaces are connected to the two RX/TX of the GNK transceiver of the

FPGA. The TX signal and the RX signal are connected to the FPGA and the optical module through the DC blocking capacitor in differential signal mode. The TX and RX data rates are up to each 6.6Gb/s per channel. The reference clock for the GTX transceiver is provided by the 125M differential clock of AC7100 FPGA core board.

Figure 3-3-1 detailed the schematic diagram of FPGA and fiber design

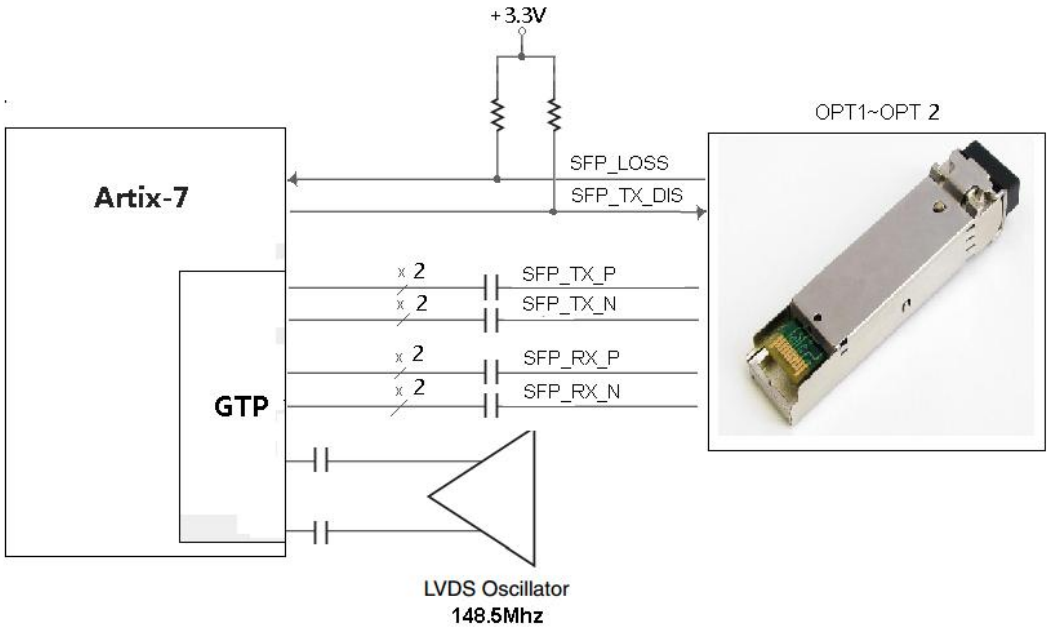


Figure 3-3-1: SFP Interface Schematic

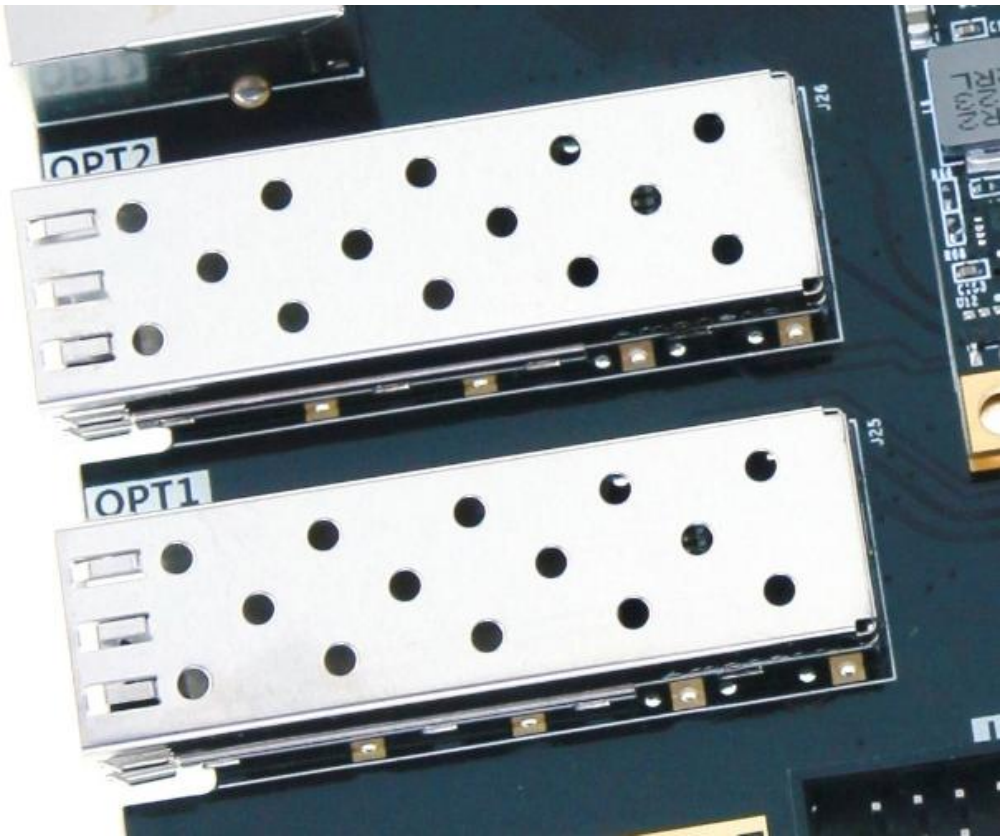


Figure 3-3-2: SFP interfaces on the Carrier Board

The 1st fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP1_TX_P	B4	SFP1 Data Transfer (Positive)
SFP1_TX_N	A4	SFP1 Data Transfer (Negative)
SFP1_RX_P	B8	SFP1 Data Receiver (Positive)
SFP1_RX_P	A8	SFP1 Data Receiver (Negative)
SFP1_TX_DIS	C22	SFP1 Optical Transfer Disable, high level valid
SFP1_LOSS	B22	SFP1 Optical LOSS, high level indicated no SFP signals received

The 2nd fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP2_TX_P	D5	SFP2 Data Transfer (Positive)
SFP2_TX_N	C5	SFP2 Data Transfer (Negative)
SFP2_RX_P	D11	SFP2 Data Receiver (Positive)
SFP2_RX_P	C11	SFP2 Data Receiver (Negative)

SFP2_TX_DIS	C20	SFP1 Optical Transfer Disable, high level valid
SFP2_LOSS	D20	SFP1 Optical LOSS, high level indicated no SFP signals received

Part 3.4: VGA display interface

The VGA display part uses the ADV7123 chip of Analog Devices, which contains three 10-bit D/A converters. It converts the input RGB digital signals into VGA video signals, and supports up to 1080p@60Hz output.

In the AX7202 carrier board, the RGB digital signal output by the FPGA is 24-bit color, and the red, green and blue colors are 8 bits each. In the schematic design, the 8-bit data of the red, green and blue output of the FPGA is connected to the upper 8 bits of the 3-channel D/A conversion data input of the ADV7123, and the low 2 position of the data input is 0. The design of the ADV7123 is shown in Figure 3-4-1.

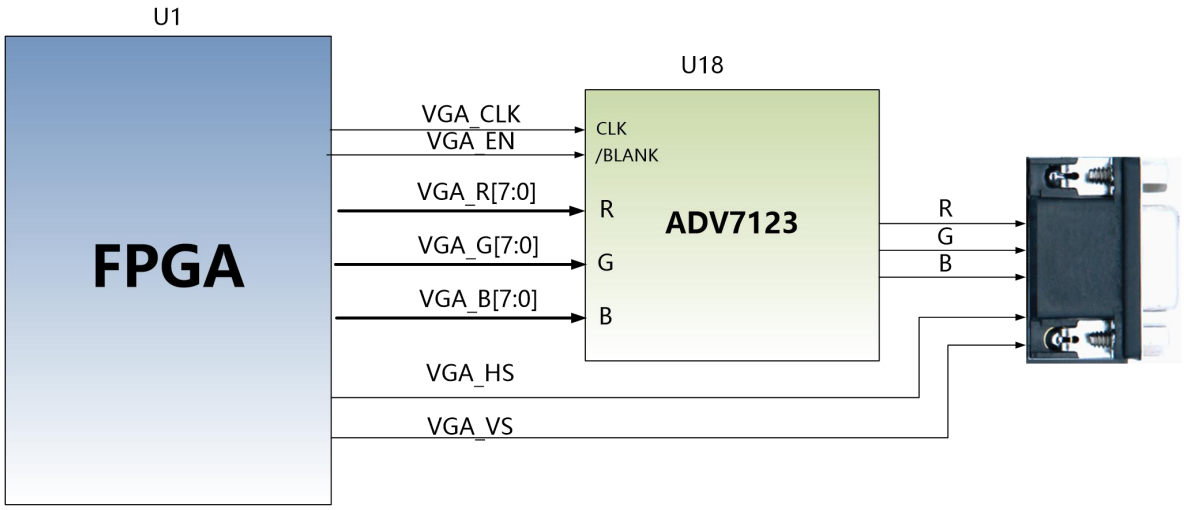


Figure 3-4-1: VGA Display Interface Schematic

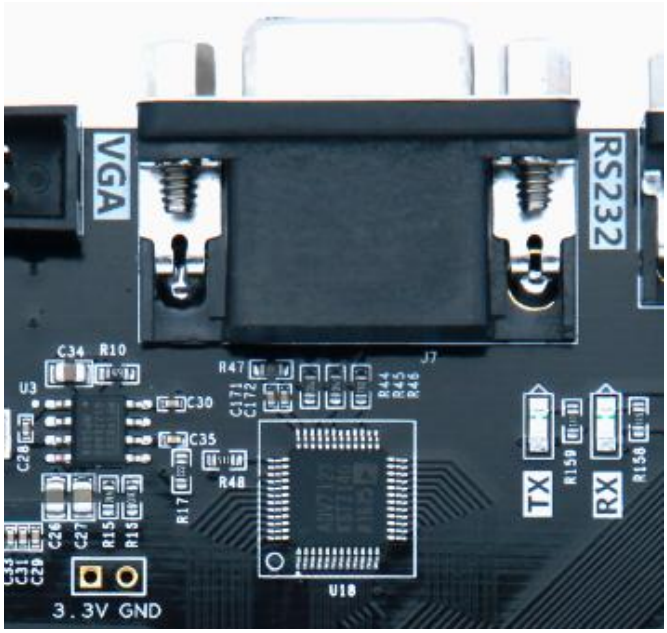


Figure 3-4-2: VGA Display Interface on the Carrier Board

VGA Pin Assignment:

Signal Name	FPGA Pin
VGA_CLK	U21
VGA_EN	AB20
VGA_HS	AA11
VGA_VS	AA10
VGA_R7	W15
VGA_R6	W16
VGA_R5	T14
VGA_R4	T15
VGA_R3	V13
VGA_R2	V14
VGA_R1	W11
VGA_R0	W12
VGA_G7	AA20
VGA_G6	AA21
VGA_G5	AB22
VGA_G4	AB21
VGA_G3	V15
VGA_G2	U15

VGA_G1	W17
VGA_G0	V17
VGA_B7	T21
VGA_B6	W21
VGA_B5	W22
VGA_B4	Y17
VGA_B3	T20
VGA_B2	AB18
VGA_B1	AA18
VGA_B0	AA19

Part 3.5: USB2.0 Interface

The AX7202 carrier board uses Cypress CY7C68013A USB2.0 controller chip to realize high-speed data communication between PC and FPGA. CY7C68013A controller fully complies with the universal serial bus protocol version 2.0 specifications, supports full speed (12Mbit/s) and low speed (1.5Mbit/s) mode. The user can perform USB2.0 data communication by connecting the USB port of the PC with the USB cable and the MINI type USB port (J6) of the development board.

The CY7C68013A is a microcontroller with integrated USB 2.0. It integrates a USB 2.0 transceiver, SIE (serial interface engine), enhanced 8051 microcontroller and programmable external interface into a single chip. The communication between CY7C68013A and other devices is very simple. It provides GPIF and FIFO modes for seamless data exchange with FPGA, DSP, ATA, UTOPIA, EPP, PCMCIA and so on.

The clock of the CY7C68013A transceiver is provided by a 24MHz crystal. The schematic diagram of the FPGA and CY7C68013A connections is shown in Figure 3-5-1.

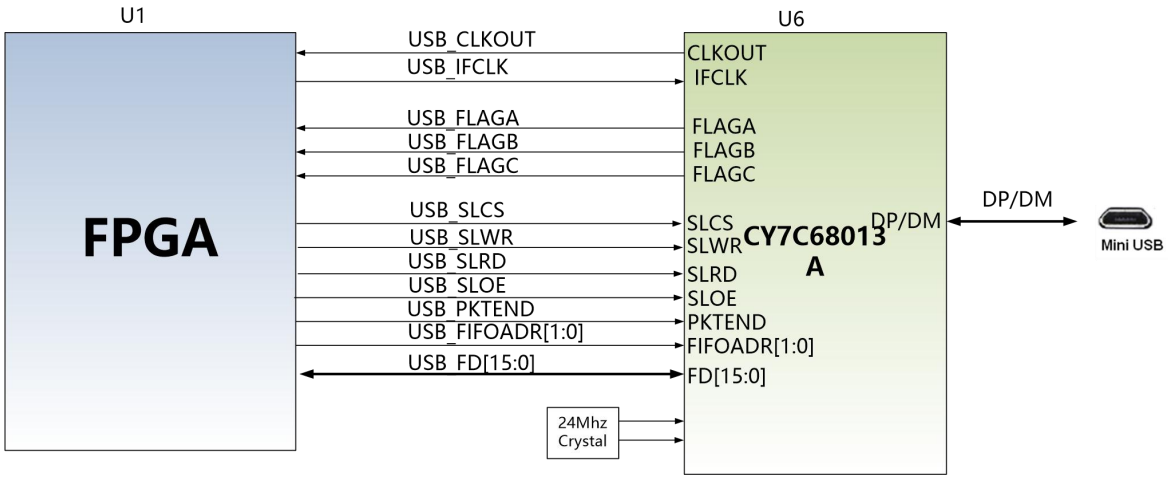


Figure 3-5-1: USB2.0 Interface schematic

The figure below is a physical diagram of the USB2.0 part, U6 is CY7C68013A, J6 is USB interface

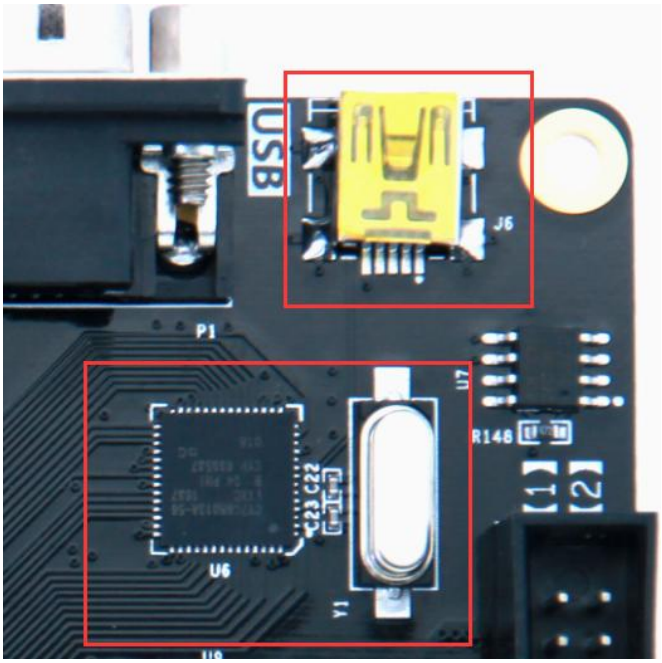


Figure 3-5-2: USB 2.0 part on the Carrier Board

USB 2.0 Pin Assignment

Signal Name	FPGA PIN	Description
USB_CLKOUT	U18	12, 24 or 48 MHz Clock Output
USB_IFCLK	Y21	Synchronous communication clock signal
USB_FLAGA	R18	Programmable slave-FIFO output status flag signal
USB_FLAGB	R14	Programmable slave-FIFO output status flag signal
USB_FLAGC	P14	Programmable slave-FIFO output status flag signal

USB_SLCS	P16	Slave FIFO chipset select
USB_SLWR	R19	Slave FIFO write signal
USB_SLRD	P19	Slave FIFO read signal
USB_SLOE	N13	Slave FIFO Data Output Enable
USB_PKTEND	P20	Commit the FIFO packet data to the endpoint
USB_FIFOADR[0]	N14	FIFO address 0
USB_FIFOADR[1]	N15	FIFO address 1
USB_FD[0]	Y22	USB data Bit0
USB_FD[1]	W20	USB data Bit1
USB_FD[2]	W19	USB data Bit2
USB_FD[3]	Y19	USB data Bit3
USB_FD[4]	Y18	USB data Bit4
USB_FD[5]	V22	USB data Bit5
USB_FD[6]	U22	USB data Bit6
USB_FD[7]	T18	USB data Bit7
USB_FD[8]	R17	USB data Bit8
USB_FD[9]	R16	USB data Bit9
USB_FD[10]	P15	USB data Bit10
USB_FD[11]	N17	USB data Bit11
USB_FD[12]	P17	USB data Bit12
USB_FD[13]	U16	USB data Bit13
USB_FD[14]	T16	USB data Bit14
USB_FD[15]	U17	USB data Bit15

Part 3.6: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted substantial research and development. In 2000, these companies launched the SD Association (Secure Digital Association), which has a strong lineup and attracted a large number of vendors. These

include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

The SD card is a very common storage device. The extended SD card supports SPI mode and SD mode. The SD card used is a MicroSD card. The schematic diagram is shown in Figure 3-6-1.

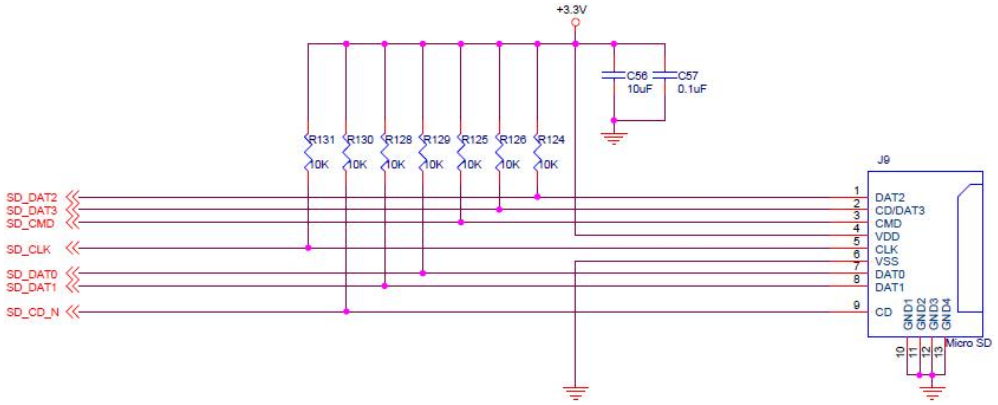


Figure 3-6-1: SD Card Schematic

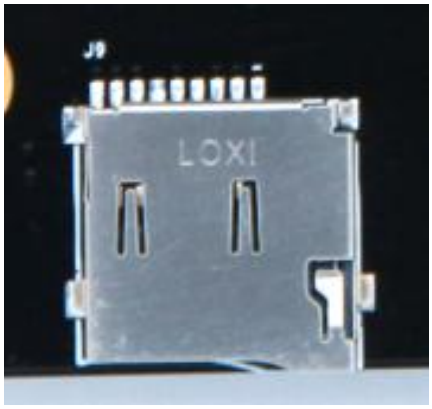


Figure 3-6-2: SD Card Slot on the Carrier Board

SD card slot pin assignment:

SD Mode	
Signal Name	FPGA PIN
SD_CLK	C14
SD_CMD	C15
SD_CD_N	B16
SD_DAT0	E17

SD_DAT1	F16
SD_DAT2	A14
SD_DAT3	A13

Part 3.7: USB to Serial Port

The development board includes the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC for serial data communication with a USB cable. The schematic diagram of the USB Uart circuit design is shown in Figure 3-7-1:

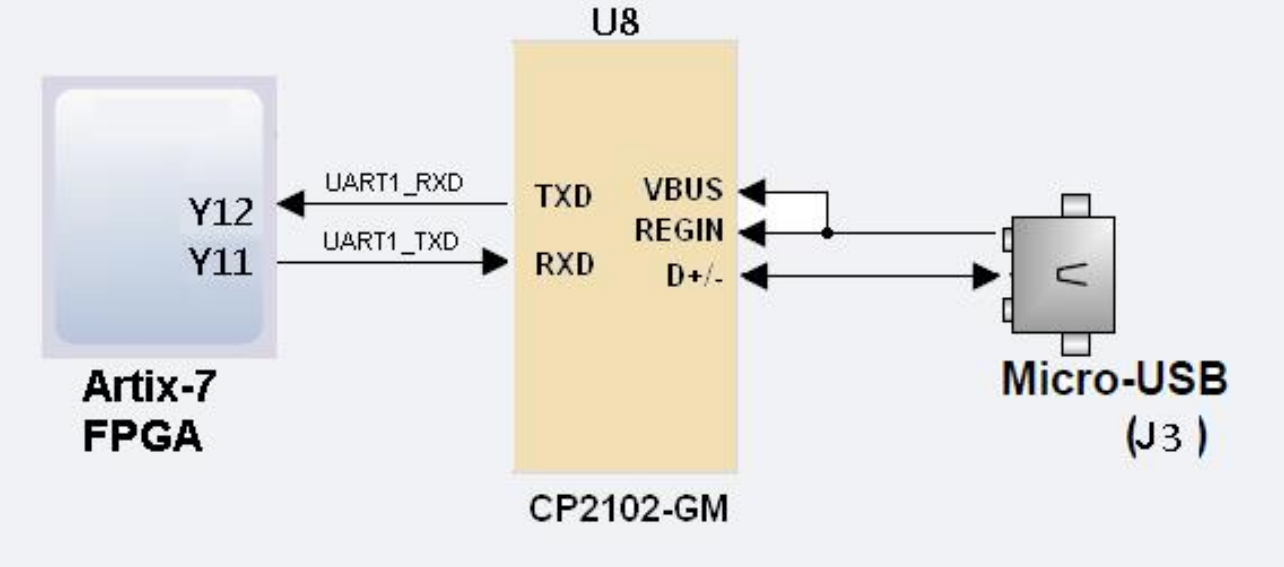


Figure 3-7-1: USB to serial port schematic

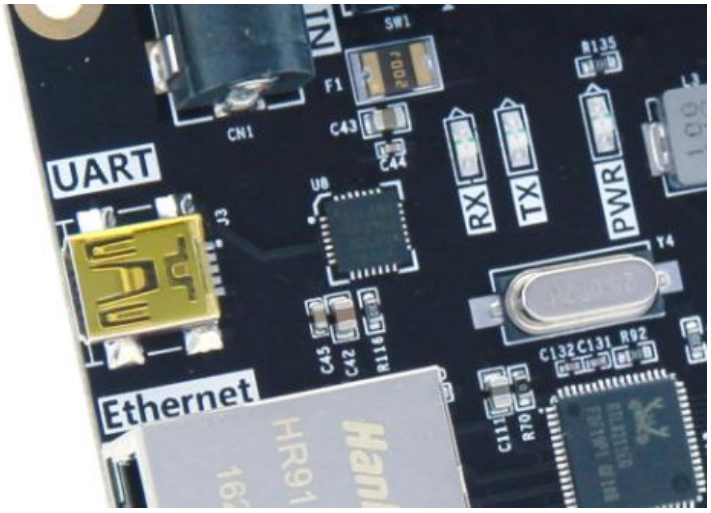


Figure 3-7-2: USB to serial port on the Carrier Board

At the same time, two LED indicators (LED7 and LED8) are set for the serial port signal, and the silkscreen on the PCB is TX and RX, indicating that the serial port has data transmission or reception, as shown in the following Figure 3-3-3

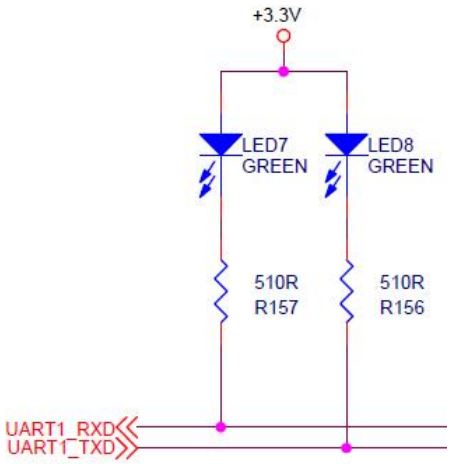


Figure 3-7-3: Serial Port communication LED Indicators Schematic

USB to serial port pin assignment:

Signal Name	FPGA PIN
UART1_RXD	Y12
UART1_TXD	Y11

Part 3.8: RS232 Interface

The AX7202 carrier board contains an RS232 male socket. Using the MAX3232 chip as a bridge for RS232 and UART level shifting, users need to prepare an RS232 serial cable (straight cable) to connect the development board to a PC or other peripheral for RS232 serial data communication. In addition, there are two LED lights on the development board to indicate the data transmission and data reception status respectively. The design diagram of the RS232 part is shown in Figure 3-8-1

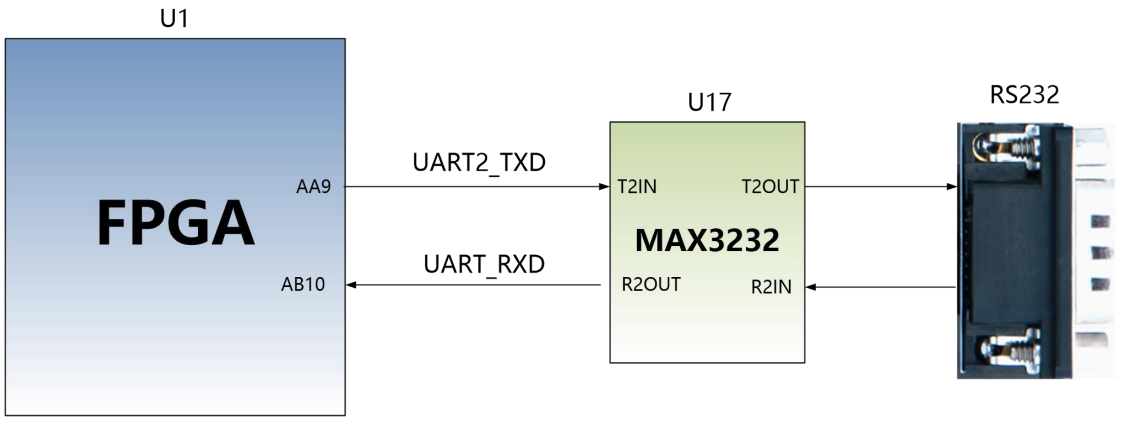


Figure 3-8-1: RS232 interface schematic

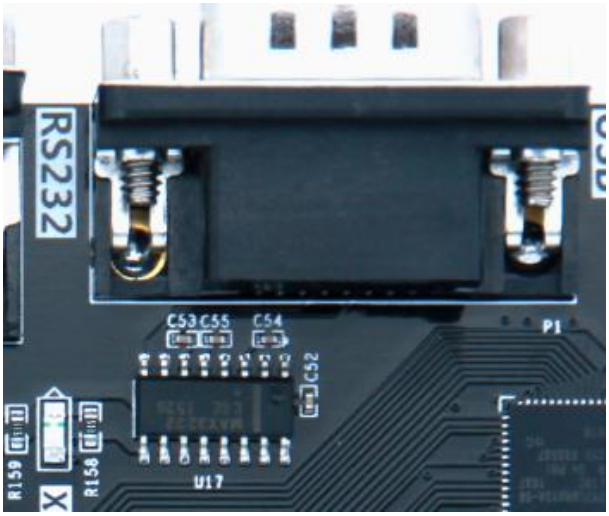


Figure 3-8-2: RS232 interface on the Carrier Board

RS232 serial port pin assignment

Signal Name	FPGA PIN
UART2_RXD	AB10
UART2_TXD	AA9

Part 3.9: EEPROM 24LC04

AX7202 carrier board contains an EEPROM, model 24LC04, and has a capacity of 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn how to communicate with the IIC bus. The I2C signal of the EEPROM is connected to the BANK14 IO port on the FPGA side. Figure 3-9-1 below shows the design of the EEPROM

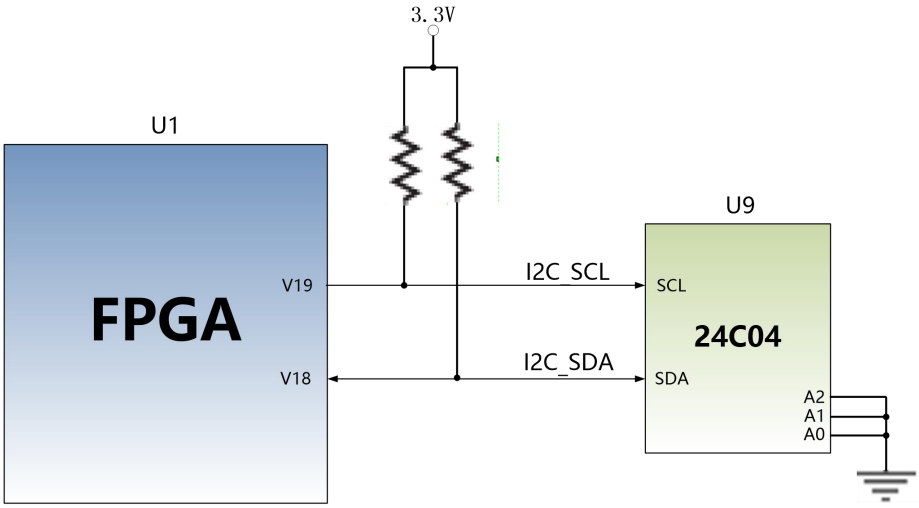


Figure 3-9-1: EEPROM Schematic

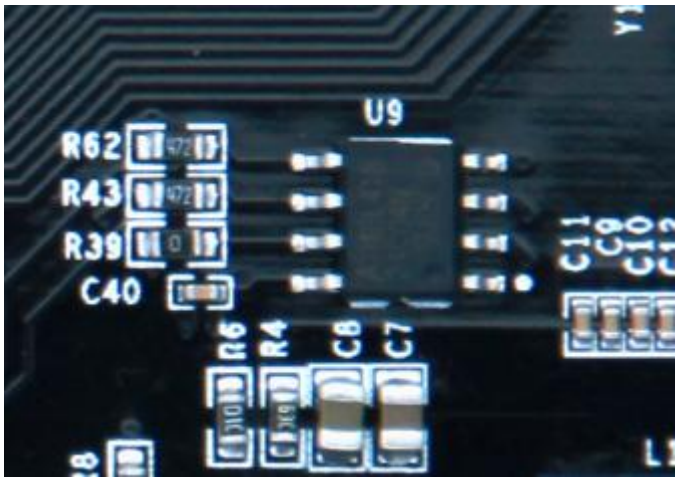


Figure 3-9-2: EEPROM on the Carrier Board

EEPROM Pin Assignment

Net Name	FPGA PIN
I2C_SCL	V19
I2C_SDA	V18

Part 3.10: Real time clock DS1302

The AX7202 carrier board contains a real-time clock RTC chip, model DS1302, which provides a calendar function up to 2099, with days, minutes, minutes, seconds and weeks. If time is needed in the system, then the RTC needs to be involved in the product. It needs to connect a 32.768KHz passive clock to provide an accurate clock source to the clock chip, so that the RTC can accurately provide clock information to the product. At the same time, in order to power off the product, the real-time clock can still operate normally. Generally, a battery is required to supply power to the clock chip. In Figure 3-10-2, the BT1 is the battery holder, and the key battery (model CR1220, voltage is 3V) is placed. After the system is turned off, the key battery can also supply power to the DS1302. This way, regardless of whether the product is powered or not, the DS1302 will operate normally without interruption and provide continuous time information. The interface signal of the RTC is also connected to the BANK16 IO port of the FPGA. Figure 3-10-1 shows the design of the DS1302:

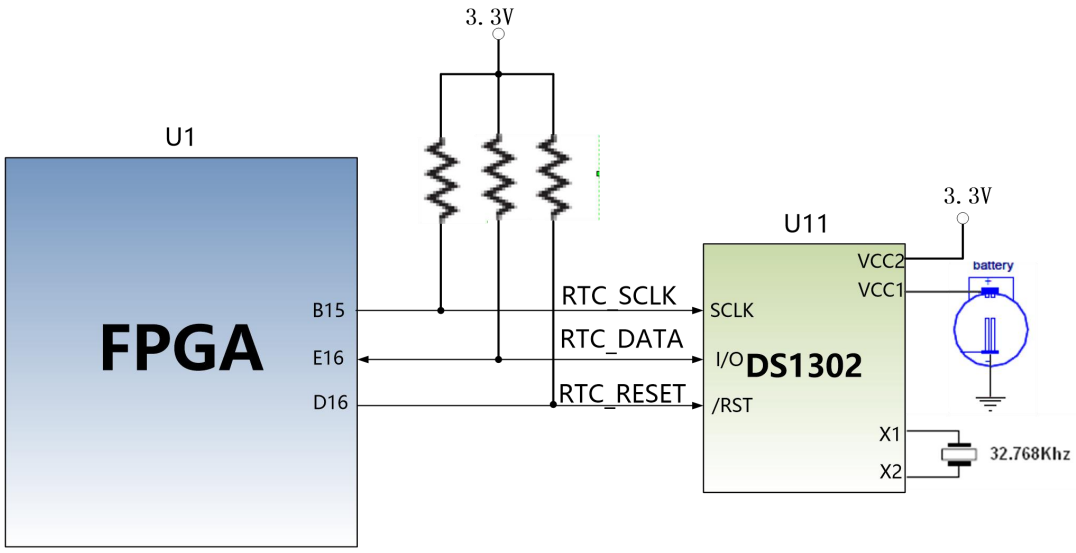


Figure 3-10-1: Real time clock DS1302 Schematic

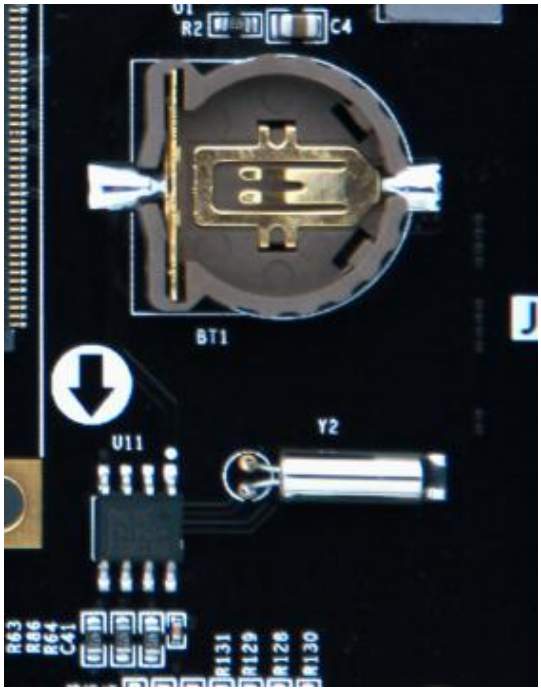


Figure 3-10-2: Real time clock DS1302 on the Carrier Board

EEPROM Pin Assignment

Net Name	FPGA PIN
RTC_SCLK	B15
RTC_DATA	E16
RTC_RESET	D16

Part 3.11: Expansion Header

The carrier board is reserved with two 2.54-mm standard 40-pin expansion ports J4 and J5, which are used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The

circuit of the expansion port (J4) is shown in Figure 3-11-1.

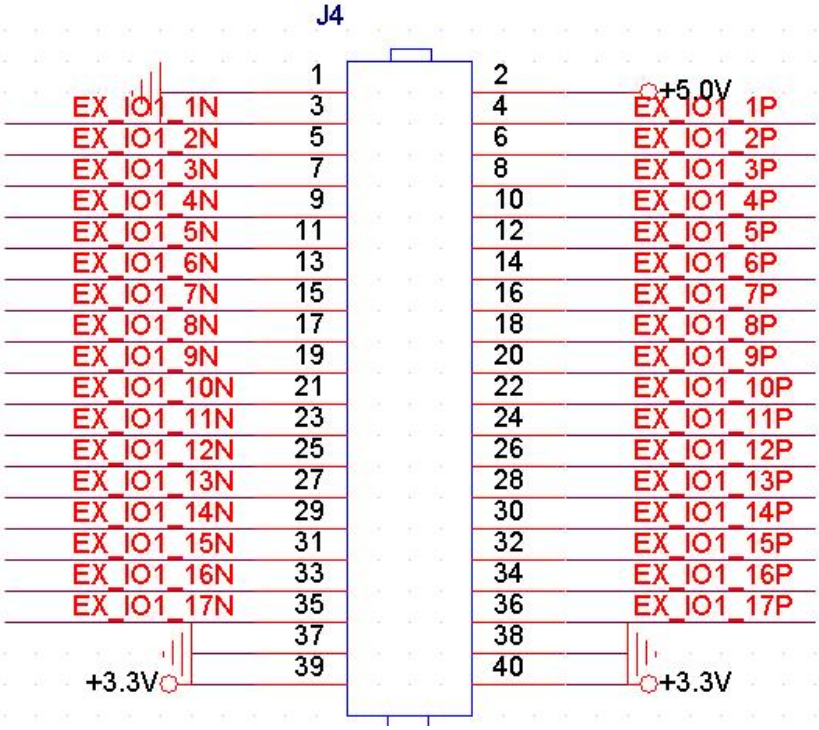


Figure 3-11-1: Expansion header J4 schematic

Figure 3-11-2: Expansion header J4 on the Carrier Board

J4 Expansion Header Pin Assignment

J4 Pin Number	FPGA Pin	J4 Pin Number	FPGA Pin
1	GND	**2**	+5V
3	K14	**4**	K13
5	H14	**6**	J14
7	H15	**8**	J15
9	G13	**10**	H13
11	J21	**12**	J20
13	G16	**14**	G15
15	H19	**16**	J19
17	G18	**18**	G17

19	J16	**20**	F15
21	K22	**22**	K21
23	H22	**24**	J22
25	G20	**26**	H20
27	G22	**28**	G21
29	D22	**30**	E22
31	D21	**32**	E21
33	A21	**34**	B21
35	M17	**36**	F21
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

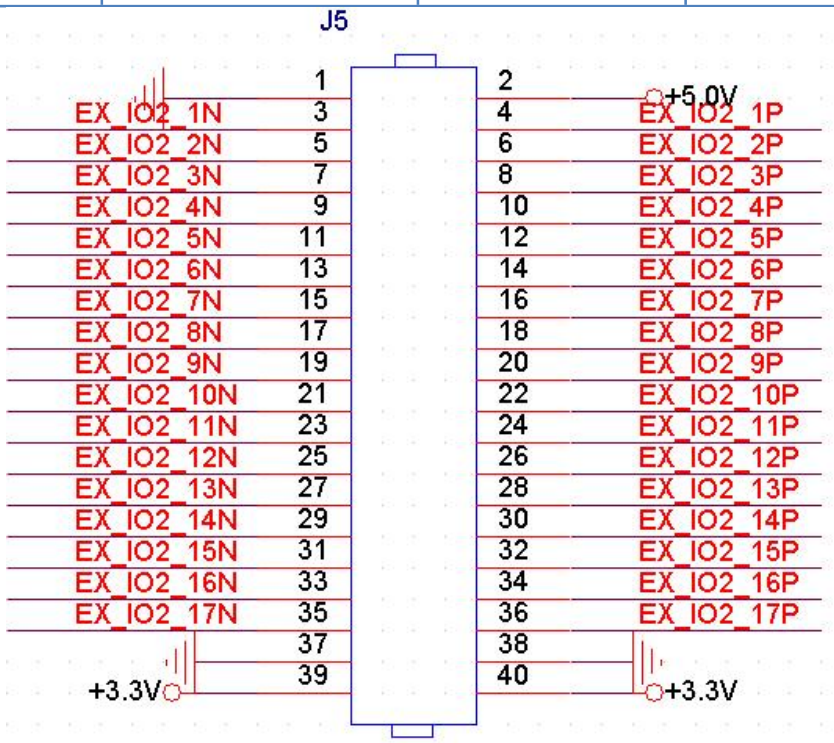


Figure 3-11-3: Expansion header J5 schematic

Figure 3-11-4: Expansion header J5 on the Carrier Board

J5 Expansion Header Pin Assignment

J5 Pin Number	FPGA Pin	J5 Pin Number	FPGA Pin
1	GND	**2**	+5V
3	AB15	**4**	AA15
5	AA14	**6**	Y13
7	AB17	**8**	AB16
9	AA16	**10**	Y16
11	AB12	**12**	AB11
13	Y14	**14**	W14
15	C19	**16**	C18
17	F14	**18**	F13
19	E14	**20**	E13
21	D15	**22**	D14
23	B13	**24**	C13
25	AB13	**26**	AA13
27	A19	**28**	A18
29	E18	**30**	F18
31	F20	**32**	F19
33	A20	**34**	B20
35	D19	**36**	E19
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Part 3.12: JTAG Interface

A JTAG interface is reserved on the AX7202 FPGA carrier board for downloading FPGA programs or firmware to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA to avoid damage of the FPGA chip.

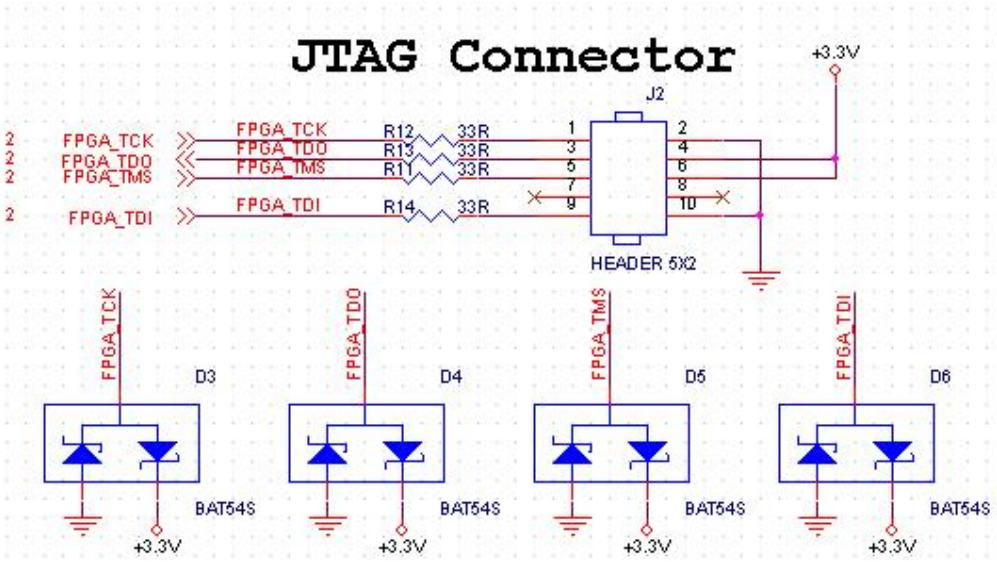


Figure 3-12-1: JTAG Interface Schematic

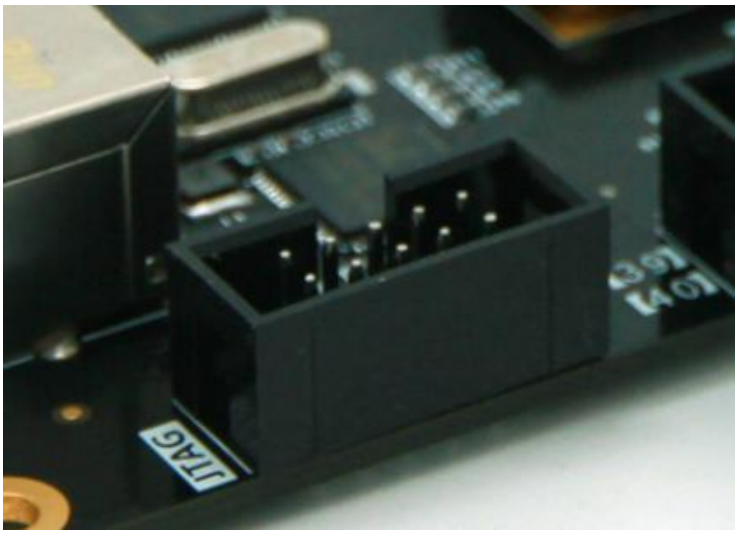


Figure 3-12-2: JTAG Interface on the Carrier Board

Be careful not to hot swap when JTAG cable is plugged and unplugged.

Part 3.13: keys

The AX7202 FPGA carrier board contains four user keys KEY1~KEY4. All keys are connected to the normal IO of the FPGA. The key is active low. When the key is pressed, the IO input voltage of the FPGA is low. When no key is pressed, The IO input voltage of the FPGA is high. The circuit of the key part is shown in Figure 3-13-1.

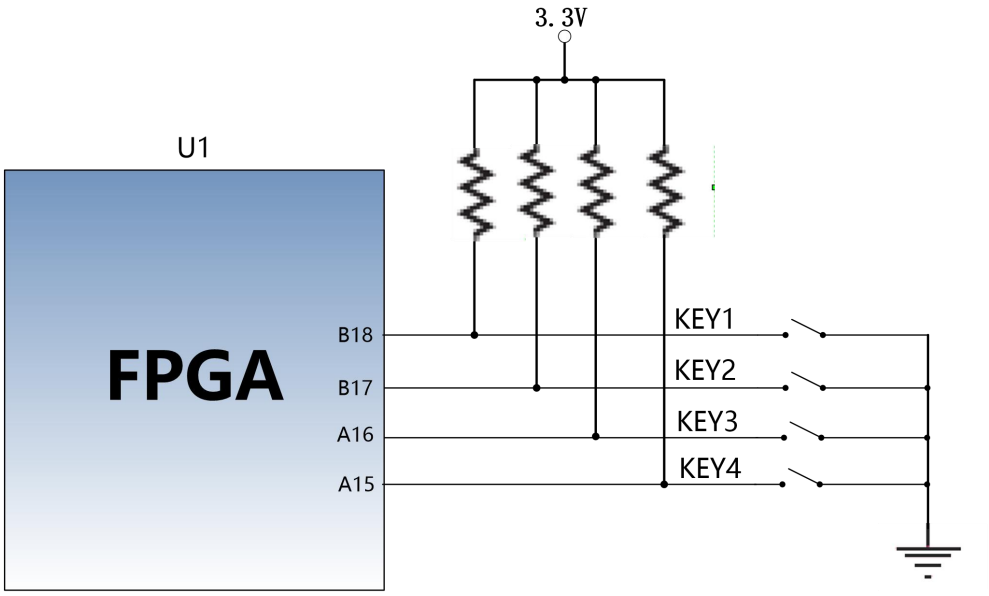


Figure 3-13-1: key Schematic

Figure 3-13-2: Four keys on the Carrier Board

keys Pin Assignment

Net Name	FPGA PIN
KEY1	B18
KEY2	B17
KEY3	A16
KEY4	A15

Part 3.14: LED Light

There are nine red LEDs on the AX7202 FPGA carrier board, one of which is the power indicator (PWR), two are USB Uart data receiving and transmitting indicators, two are RS232 data receiving and transmitting indicators, and four are users LED lights (LED1~LED4). When the board is powered on, the power indicator will light up; User LED1~LED4 are connected to the normal IO of the

FPGA. When the IO voltage connected to the user LED is configured low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be extinguished. The schematic diagram of the user LEDs hardware connection is shown in Figure 3-14-1.

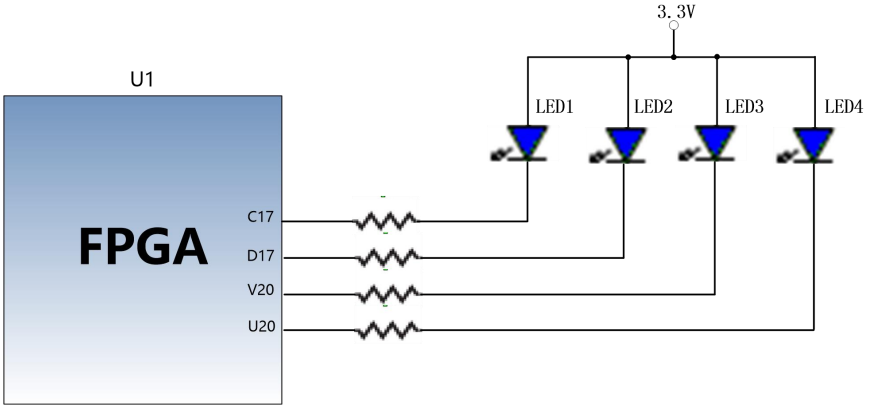


Figure 3-14-1: The User LEDs Schematic

Figure 3-14-2: The User LEDs on the Carrier Board

Pin assignment of user LED lights

Signal Name	FPGA PIN
LED1	C17
LED2	D17
LED3	V20
LED4	U20

Part 3.15: Power Supply

The power input voltage of the AX7202 FPGA development board is DC12V. The carrier board is converted into +5V and +3.3V two-way power supply through one DC/DC power supply chip. In addition, the +5V power supply on the carrier board supplies power to the core board through the

inter-board connector. The power supply design on the expansion is shown in Figure 3-15-1.

Because the +5V power supply supplies power to the AC7Z035 FPGA core board through the inter-board connector, the DCDC power supply has a current output of 6A, and the other three power supply current outputs are 2A

The schematic diagram of the power supply design on the AX7Z0350 FPGA development board is shown in Figure 3-15-1

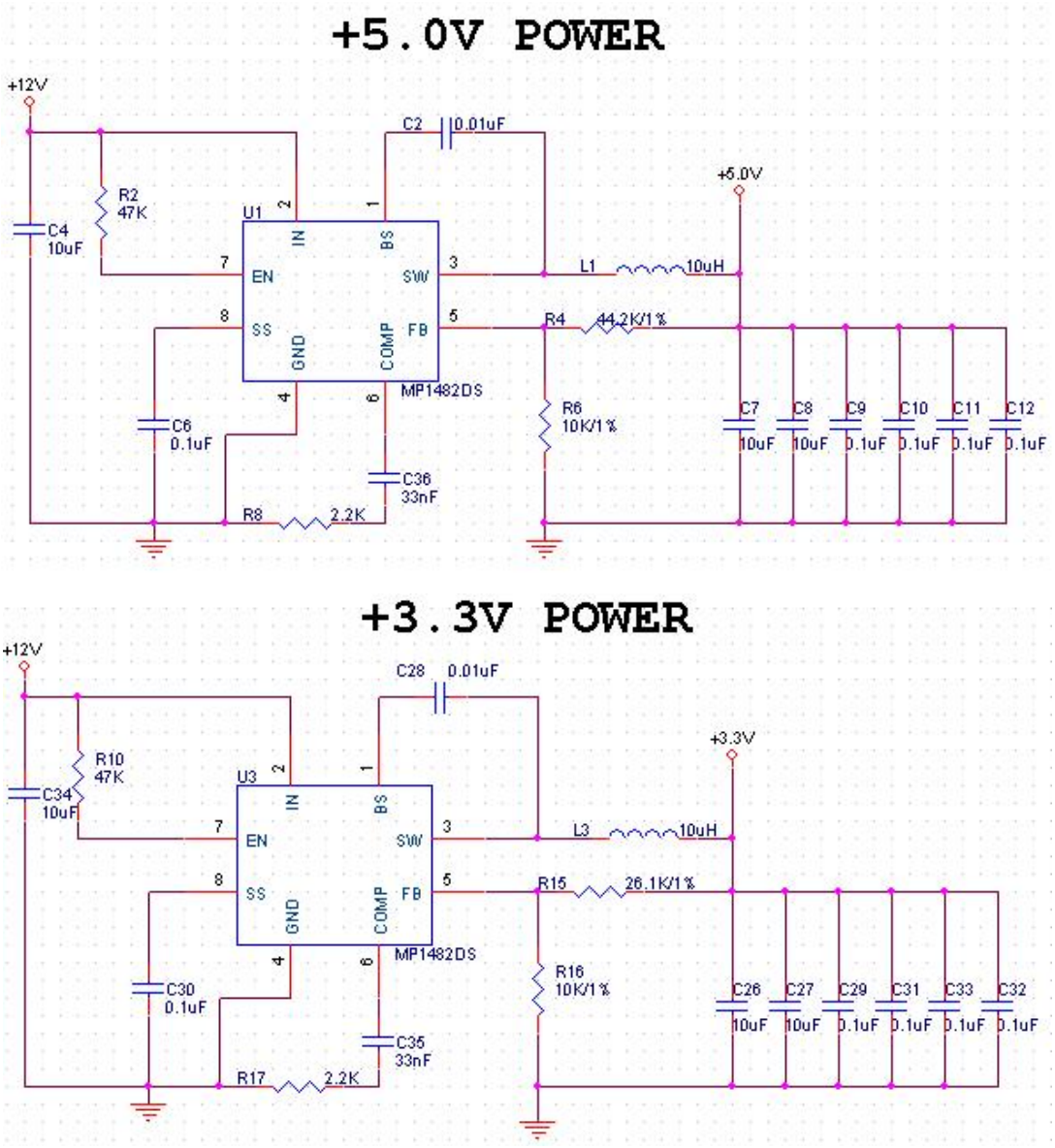


Figure 3-15-1 Power Design Schematic on the Carrier Board

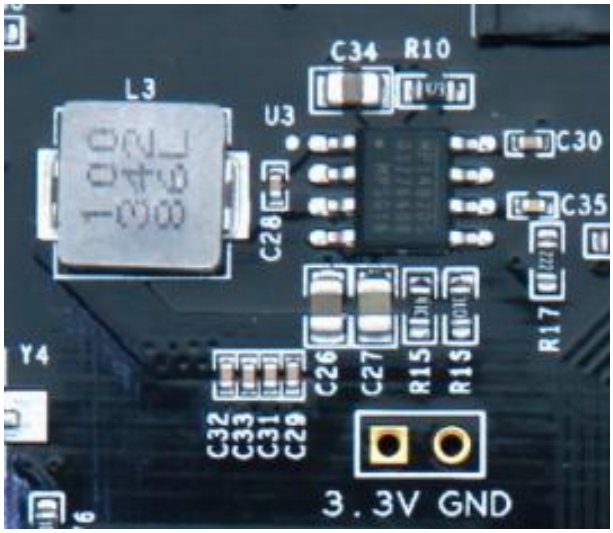


Figure 3-15-2: +3.3V Power circuit on the Carrier Board

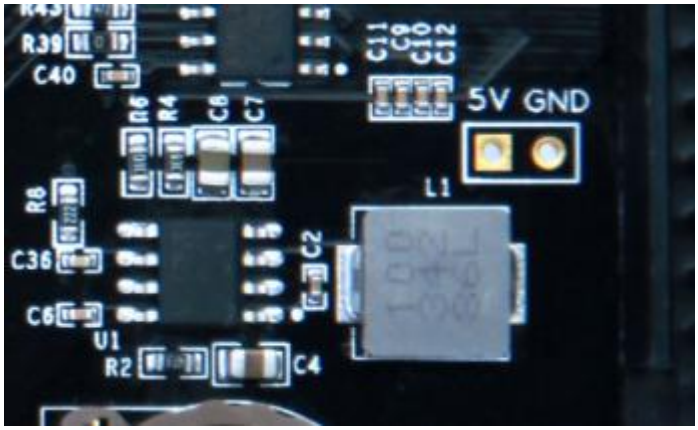


Figure 3-15-3: +5V Power circuit on the Carrier Board