Spartan-6 FPGA Development Board AX516 User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2019-04-28	Rachel Zhou	First Release

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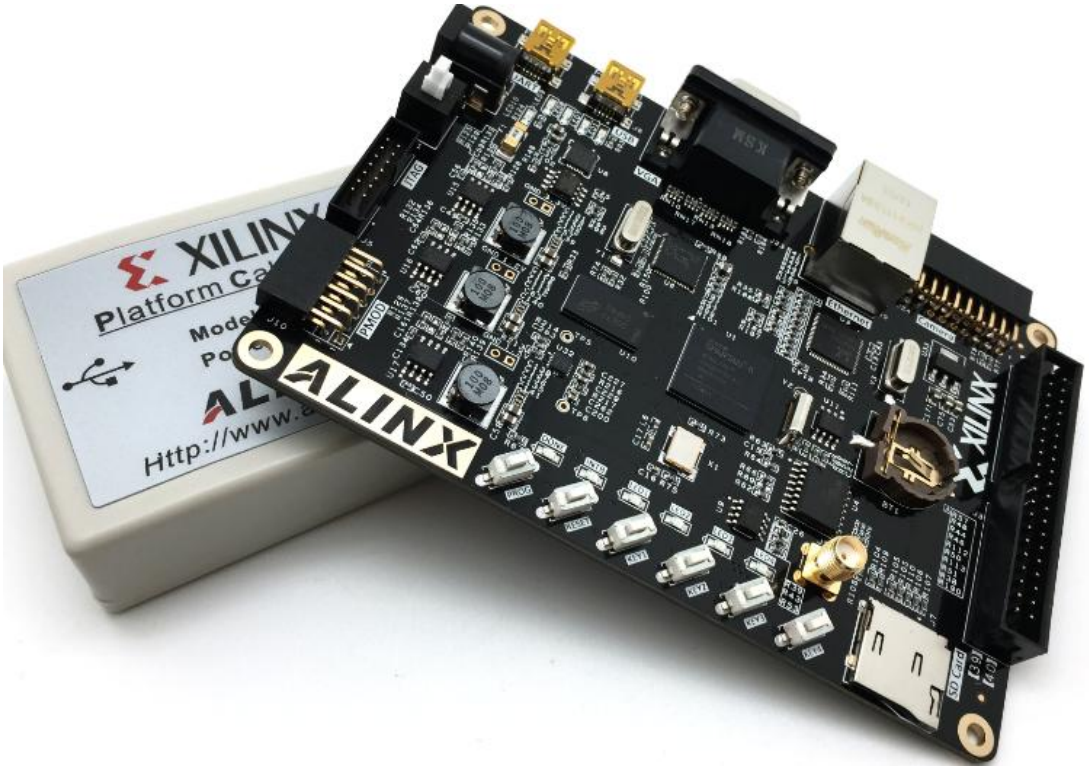
The AX516 FPGA development board uses the XILINX SPARTAN6 family chips, model XC6SLX16-2CSG324. As a core processor, FPGA has rich hardware resources and peripheral interfaces. In the design, adhere to the "exquisite, practical, simple" design concept, it is very suitable for software radio, industrial control, multimedia applications, IC verification, parallel computing and other project development, and it can also be applied to college teaching, FPGA training, personal research learning and DIY, etc.



The Photograph of FPGA Board

Part 1: FPGA Development Board Introduction

The FPGA chipset is Xilinx Spartan-6 XC6SLX16 device in FBGA324 package, the feature summary of this FPGA device are listed below:

Device	Logic Cells[1]	Configurable Logic Blocks (CLBs)			DSP48A1 Slices[3]	Block RAM Blocks		CMTs[5]	Memory Controller Blocks (Max)[6]	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices[2]	Flip-Flops	Max Distributed RAM (Kb)		18 Kb[4]	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540

Table 1-1: The Feature Summary of FPGA Device

The main resources and features are listed (see Table 1-2):

Parameter	Value
Logic Cells	14579
DSP48 Slices （18 x 18 multiplier, an adder, and accumulator）	32
Configurable Logic Blocks(CLBs)	136Kb
Block RAM Blocks	576Kb
CMTs	2
MAX User I/O	218
Core Power Supply	1.15V-1.25V (recommended 1.2V)
Operation Temperature	0-85℃

Table 1-2: The Main Resources and Feature of Xilinx Spartan6 XC6SLX9

The layout of the board that indicates the location of the connector and key components, provide a quickly overview of AX516 board (see Figure 1-2)

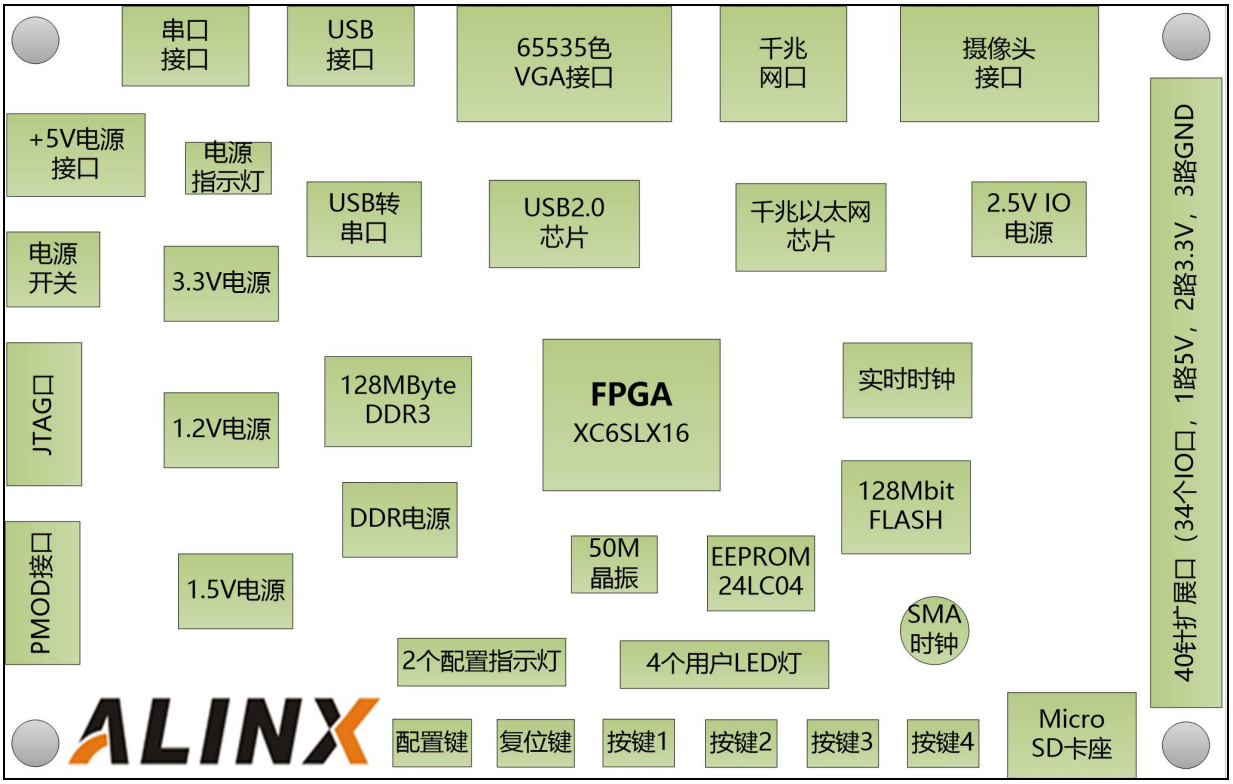


Figure 2-1: The Layout of the AX516 board

Through this diagram, we can see the functions that the development platform can achieve.

- +5V power input, maximum 2A current protection
- A large 128Mbyte high-speed DD3 SDRAM can be used as a buffer for data or as a memory for Microblaze
- A 128Mbit QSPI FLASH that can be used as a storage for FPGA configuration files and user data
- One-way 10/100M/1000M Ethernet RJ-45 interface for Ethernet data exchange with computers or other network devices;
- One-way high-speed USB2.0 interface, can be used for USB2.0 high-speed communication between FPGA development board and PC
- One USB Uart interface for serial communication with PC or external devices

- A camera module interface that can connect 5 million OV5640 camera
- One-port VGA interface, VGA interface is 16bit, can display 65,536 colors, can display color pictures, etc
- A piece of RTC real time clock with battery holder, battery model CR1220
- One piece of IIC interface EEPROM 24LC04
- 4 red user LEDs
- 4 independent user buttons
- On-board 50M active crystal oscillator provides stable clock source for FPGA development board
- 1-Way 40-pin ALINX expansion port (0.1”inch), 34 IO ports, one 5V power supply, two 3.3V power supplies, three GND. Two expansion modules can be connected at the same time, such as expansion modules such as 4.3-inch TFT module and AD/DA module.
- Reserved JTAG port for FPGA debugging and program curing
- One way Micro SD card holder, support SD mode and SPI mode
- Reserve a 2.5V power supply, optional IO voltage 3.3V and 2.5V for FPGA
- One SMA interface for input or output of an external clock

Part 2: Structure Diagram

The size of the development board is a compact 130mm x 90mm, and the PCB is designed with an 8-layer board. There are 4 screw positioning holes around the FPGA board for fixing the development board. The hole diameter of the positioning hole is 3.3mm (diameter)

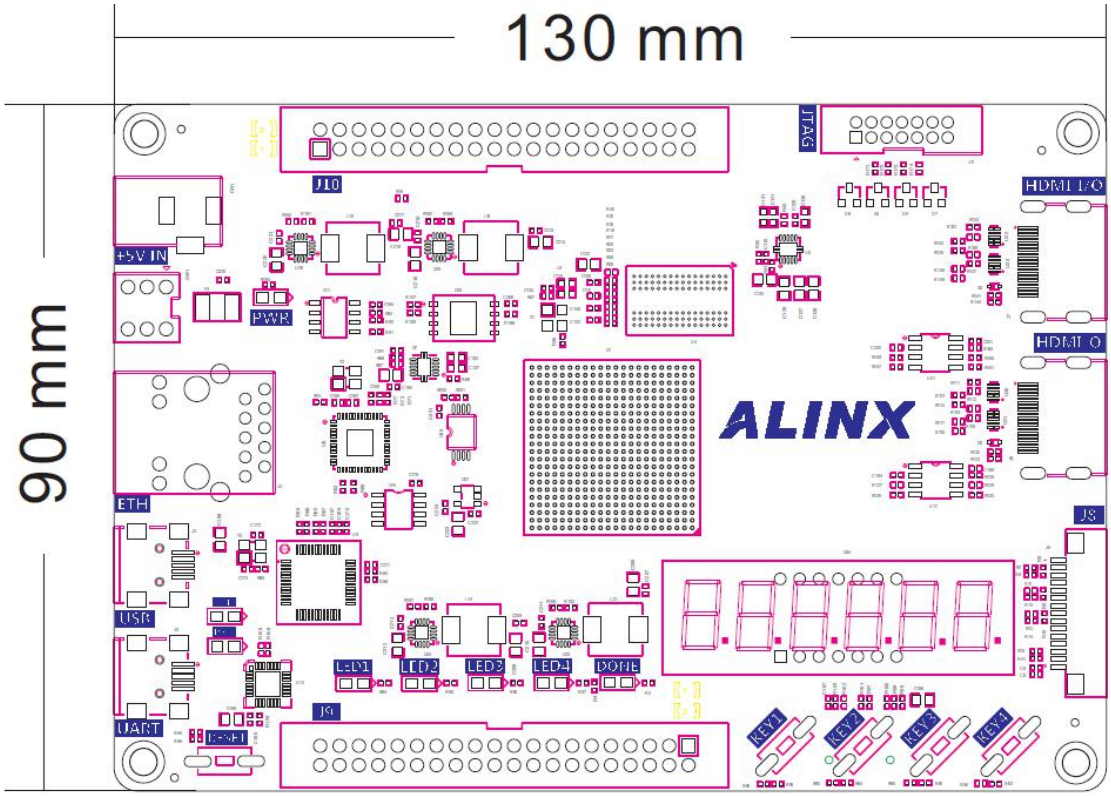


Figure 2-1: Structure Diagram

Part 3: Power

The FPGA development board power supply input voltage is DC5V. The power supply design diagram on the development board is as Figure 3-1:

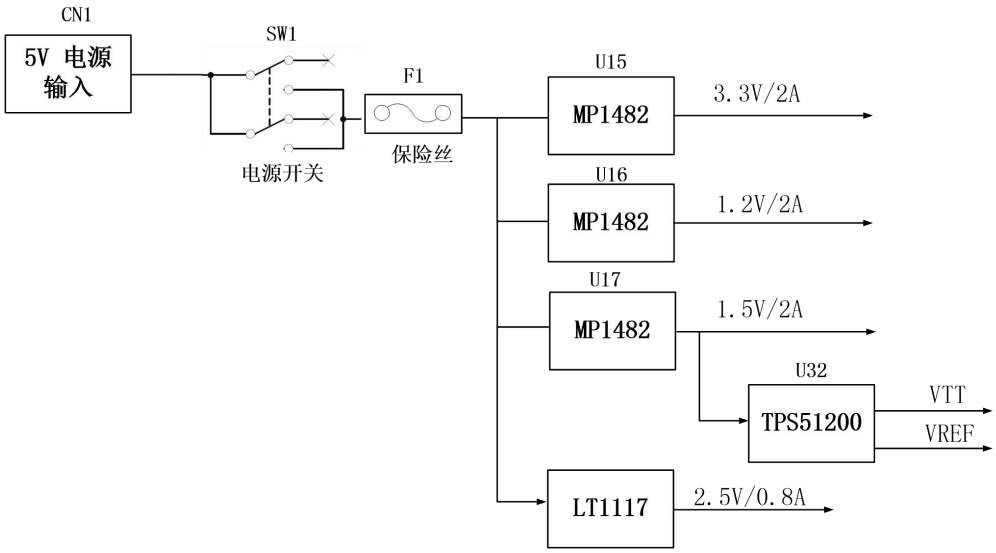


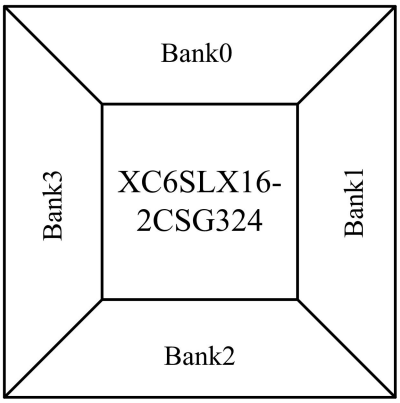
Figure 3-1: Block Diagram of Power Design

The development board is powered by +5V, and is converted into +3.3V, +1.2V, +1.5V three-way power supply through three-way DC/DC power supply chip MP1482. It generates +2.5V power supply through one LDO LT1117, and VTT and VREF voltages (1.5V) required for DDR3 is generated by TPS51200 of TI. The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.2V	FPGA Core Voltage
+3.3V	FPGA, Ethernet, Serial port, RTC, FLASH, EEPROM, USB 2.0 and SD Card
+1.5V	DDR3, Bank3 of FPGA
VREF,VTT	DDR3
+2.5V	FPGA Bank2 optional

The IO voltage of FPGA BANK2 can be selected by two 0 ohm resistors (R158, R159) on the board. When R158 is installed and R159 is not installed, the IO level of Bank2 is 3.3V. When R158 is not installed and R159 is installed. the IO level of Bank2 is 2.5V

FPGA BANK voltage distribution detailed as table 3-1:



BANK	Function	Voltage	Description
BANK0	VGA, USB2.0, PMOD, UART	3.3V	
BANK1	SD Card, Camera, Ethernet, VGA	3.3V	
BANK2	Extend IO，QSPI FLASH, LED, KEY	3.3V/2.5V	
BANK3	DDR3, Reset Button	1.5V	

Table 3-1: FPGA BANK voltage distribution

When designing the PCB, we used a 6-layer PCB and reserved a separate Power layer and GND layer, which ensures the FPGA development board has very good stability. On the PCB we have reserved test points for each power supply so that the user can confirm the voltage on the board.

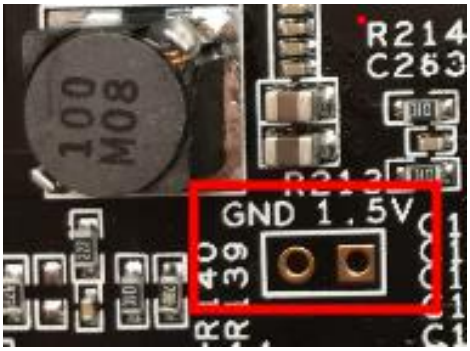


Figure 3-2: The Test Point of Power Voltage

Part 4: FPGA Chip

As mentioned earlier, the FPGA model we use is XC6SLX16-2CSG324, which belongs to Xilinx Spartan-6. This model is a BGA package with 324 pins. Again, explain the definition of the FPGA pin. Many people use FPGAs that are not BGA-packaged, such as 144-pin, 208-pin FPGA chips. Their pin definitions are made up of numbers, such as 1 to 144, 1 to 208, etc., and when we use BGA packages. After the chip, the pin name becomes in the form of letters + numbers, such as E3, G3, etc., so when we look at the schematic, we see the letters + numbers, which represent the pins of the FPGA. Having said this, let's look at the functions of the various parts of the FPGA.

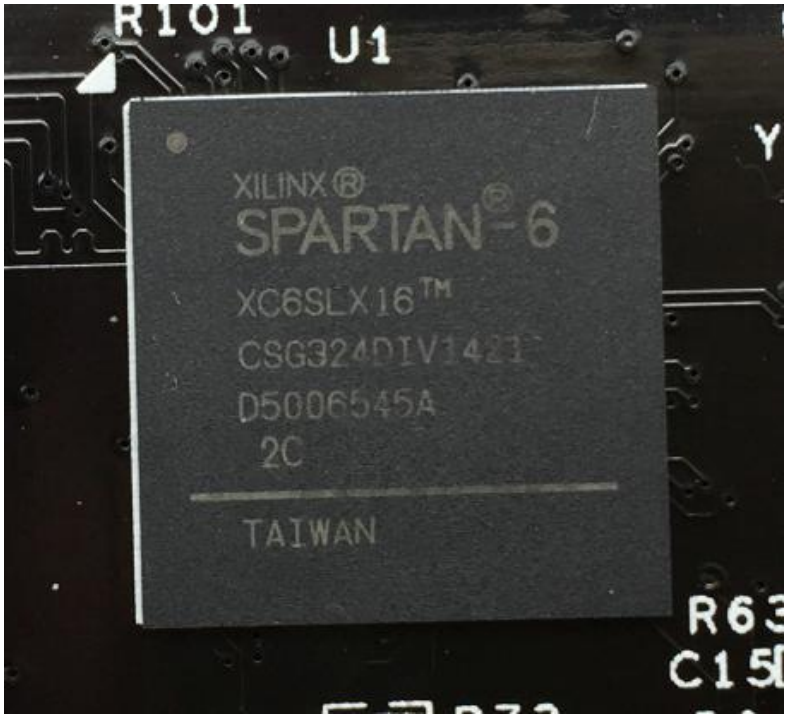


Figure 4-1: FPGA Chipset

Part 4.1: JTAG Interface

First, let's talk about the FPGA configuration and debug interface: the JTAG interface. The function of the JTAG interface is to download the compiled program (.bit) to the FPGA or download the FLASH configuration program (.mcs) to the SPI FLASH. After the Bit file is downloaded to the FPGA, it will be lost after power-off. It needs to be powered on and downloaded again. However, after downloading the MCS file to FLASH, it will not be lost after power-off. After power-on, the FPGA will read the configuration file in FLASH and run it.

The hardware design of JTAG connector is showed as Figure 4-2, JTAG interface includes four signals (TCK,TDO,TMS,TDI). these four signals connects between FPGA device and JTAG connector with 33ohm resistors, the 33ohm resistors will protect FPGA device to avoid damage。

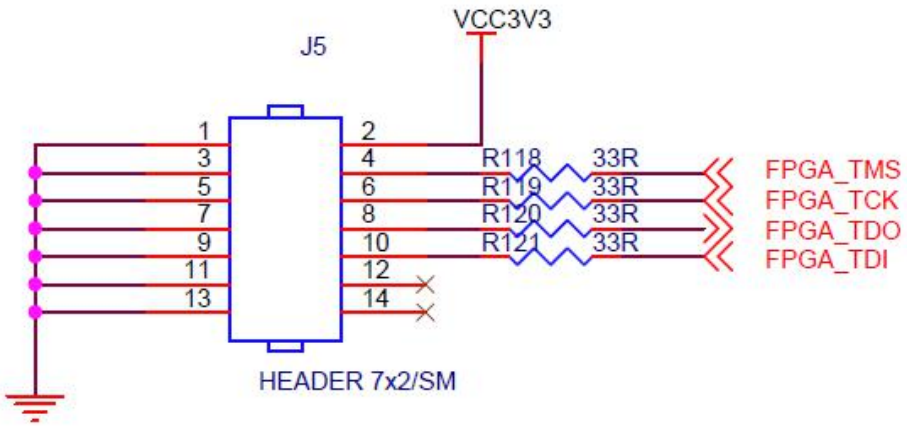


Figure 4-2: Hardware Design of JTAG Connector

JTAG connector is 14pin connectors, the pin pitch is 2.0mm.

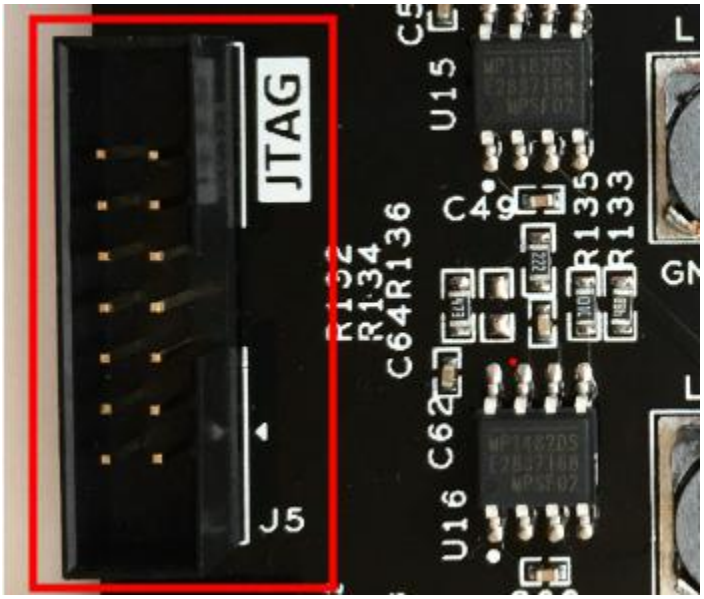


Figure 4-3: Onboard JTAG Connector

Part 4.2: FPGA Power Supply

Next, let's talk about the power supply pin part of the FPGA, including the power supply pin of each bank, the core voltage pin and the auxiliary voltage pin.

VCCINT is the FPGA core power supply pin, connected to 1.2V; VCCAUX is the FPGA auxiliary power supply pin, can be connected to 3.3V or 2.5V, here connected to 3.3V; VCCINT and VCCAUX connection as shown in Figure 3-4

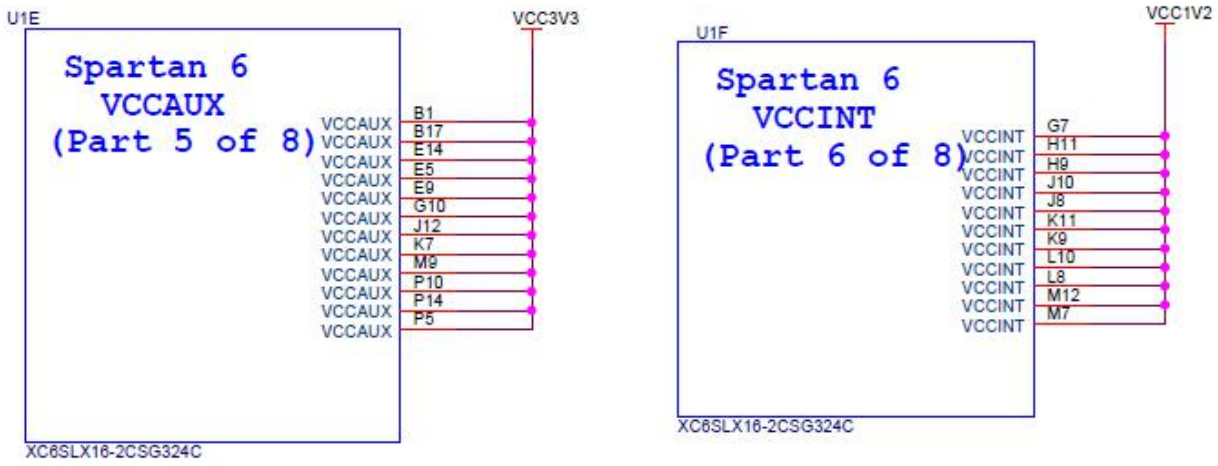


Figure 4-4: FPGA Power Supply

VCCIO is the supply voltage of each BANK of the FPGA. VCCIO0 is the power supply pin of BANK0 of FPGA. Similarly, VCCIO1~VCCIO3 are the power supply pins of BANK~BANK3 of FPGA respectively. In the FPGA development board, VCCIO0 and VCCIO1 are connected to 3.3V, which means that the corresponding FPGA pins are 3.3V input and output. VCCIO2 is also connected to 3.3V by default, but the user can select 2.5V by changing the resistance (R158 is not installed, R159 is installed). Because the pin of BANK3 is connected to a DDR3, VCCIO3 is connected to 1.5V. Figure 3.5 shows the connection diagram of VCCIO of BANK2. Figure 3-5 is a connection diagram of VCCIO of BANK2.

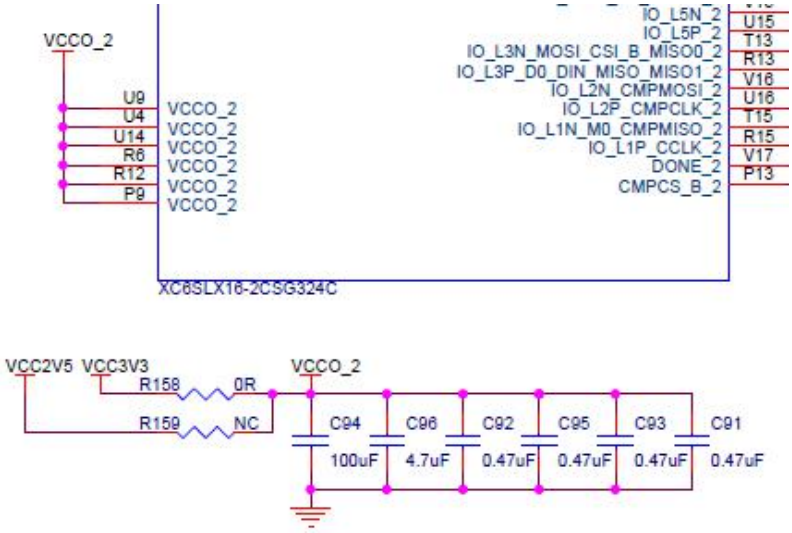


Figure 4-5: FPGA power supply VCCIO pin

Part 5: 50Mhz Clock

Figure 5-1 is the clock circuit of the FPGA development board, an 50Mhz crystal oscillator provides the clock source for the whole board. The output of the crystal oscillator is connected to the FPGA global clock (GCLK Pin V10). This GCLK can be used to drive the user's logic circuit inside the FPGA. Users can configure the internal PLLs and DCMs of FPGA to achieve higher clocks.

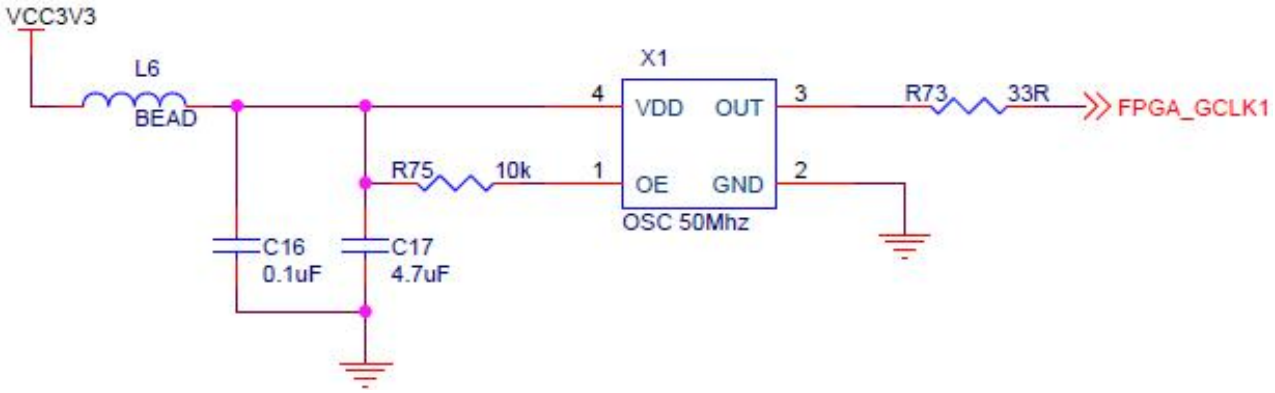


Figure 5-1: 50Mhz Crystal Oscillator

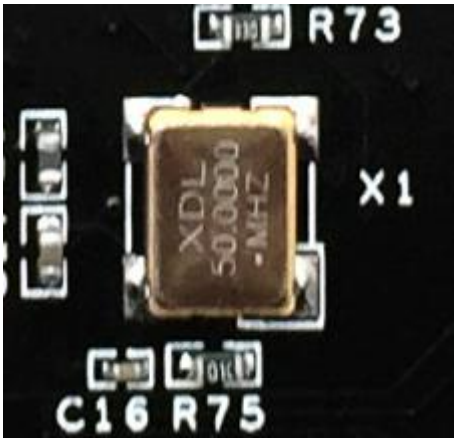


Figure 5-2: 50Mhz crystal oscillator onboard

Net Name	FPGA PIN
FPGA_GCLK	V10

Table 5-1: Clock Pin Assignment

Part 6: QSPI Flash

The AX516 FPGA development board is equipped with one 128MBit QSPI FLASH, and the model is W25Q128 which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, core application code and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 6-1.

Position	Model	Capacity	Factory
U6	N25Q256BV	32M Bit	Winbond

Table 6-1: QSPI FLASH Specification

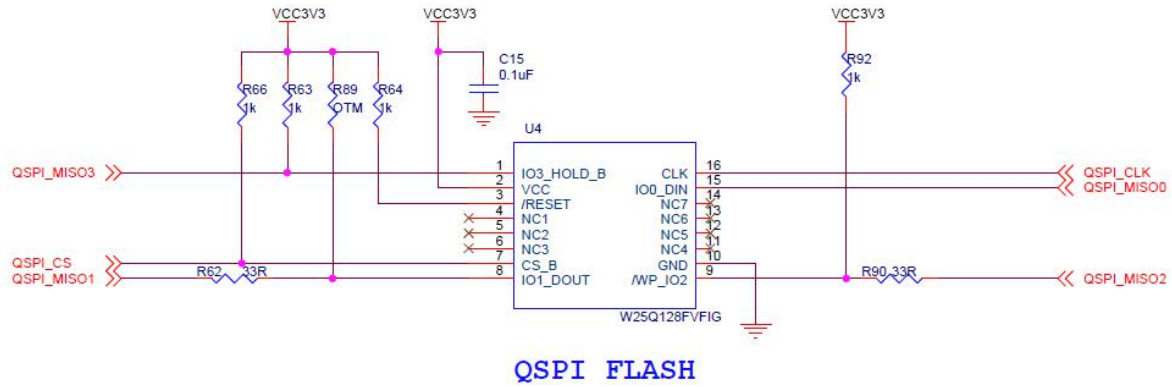


Figure 6-1: QSPI Flash Schematic

QSPI Flash pin assignments:

Pin Name	FPGA Pin
QSPI_CLK	R15
QSPI_CS	V3
QSPI_MISO0	T13
QSPI_MISO1	R13
QSPI_MISO2	T14
QSPI_MISO3	V14

Part 7: DDR3 DRAM

The AX516 FPGA development board is equipped with one high speed DDR3 DRAM, Model：MT41J64M16LA-187E, Capacity 128MByte (64M*16bit); 16bit bus. The FPGA and DDR3 DRAM on the development board are connected to the IO of BANK3. The Spartan6 FPGA has a hard DDR3 controller MCB inside. The configuration can make the MCB and DDR3 read and write speeds reach 666Mb/s. The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of

DDR3.

Figure 7-1 detailed the DDR3 DRAM hardware connection

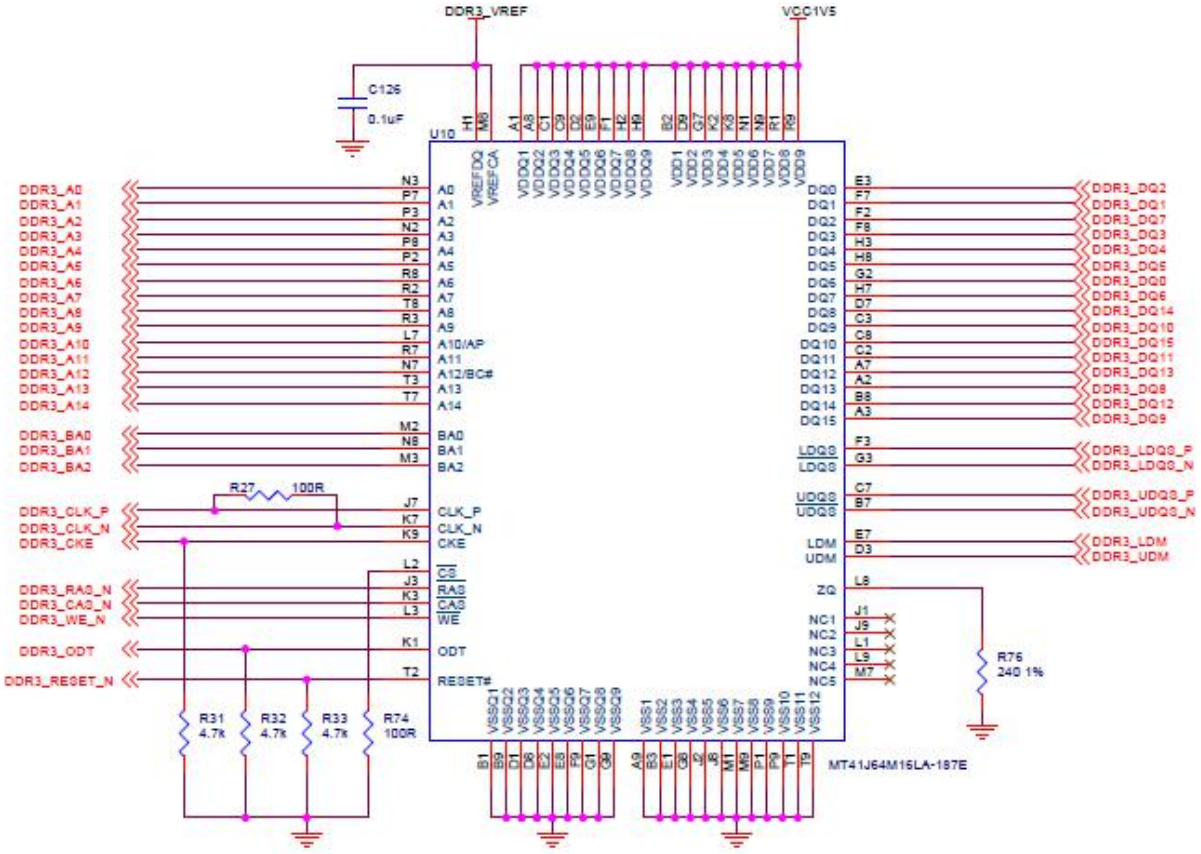


Figure 7-1: DDR3 DRAM Hardware Connection

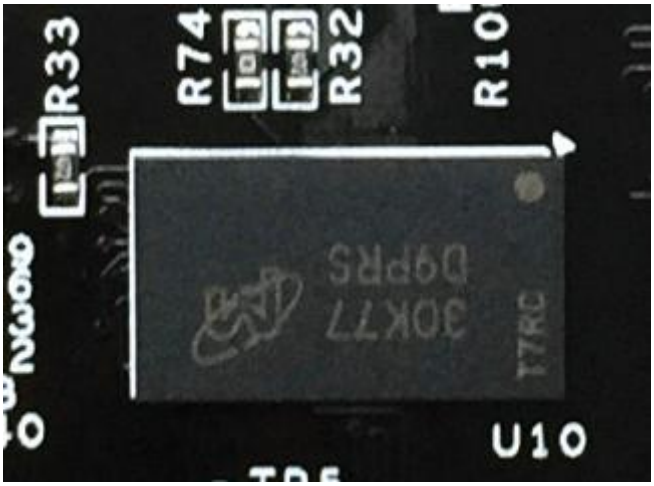


Figure 7-2: DDR3 DRAM on the FPGA Board

DDR3 DRAM Pin Assignment：

Pin Name	FPGA Pin
DDR3_LDQS_P	L4
DDR3_LDQS_N	L3
DDR3_UDQS_P	P2
DDR3_UDQS_N	P1
DDR3_DQ[0]	L2
DDR3_DQ [1]	L1
DDR3_DQ [2]	K2
DDR3_DQ [3]	K1
DDR3_DQ [4]	H2
DDR3_DQ [5]	H1
DDR3_DQ [6]	J3
DDR3_DQ [7]	J1
DDR3_DQ [8]	M3
DDR3_DQ [9]	M1
DDR3_DQ [10]	N2
DDR3_DQ [11]	N1
DDR3_DQ [12]	T2
DDR3_DQ [13]	T1
DDR3_DQ [14]	U2
DDR3_DQ [15]	U1
DDR3_LDM	K3
DDR3_UDM	K4
DDR3_A[0]	J7
DDR3_A [1]	J6
DDR3_A [2]	H5
DDR3_A [3]	L7
DDR3_A [4]	F3
DDR3_A [5]	H4
DDR3_A [6]	H3
DDR3_A [7]	H6
DDR3_A [8]	D2

DDR3_A [9]	D1
DDR3_A [10]	F4
DDR3_A [11]	D3
DDR3_A [12]	G6
DDR3_A [13]	F6
DDR3_BA [0]	F2
DDR3_BA [1]	F1
DDR3_BA [2]	E1
DDR3_RAS_N	L5
DDR3_CAS_N	K5
DDR3_WE_N	E3
DDR3_ODT	K6
DDR3_RESET_N	E4
DDR3_CLK_P	G3
DDR3_CLK_N	G1
DDR3_CKE	H7

Part 8: EEPROM 24LC04

The development board contains an EEPROM, model 24LC04, and its capacity is 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn the communication method of the IIC bus. EEPROM is generally used in the design of instruments and meters, Used as a storage for some parameters, power-off is not lost. This chip is simple to operate and has a very high cost performance, so although the capacity ratio is high, the price is very cheap, which is a good choice for those products that are costly. Figure 8-1 detailed the EEPROM 24LC04 schematic:

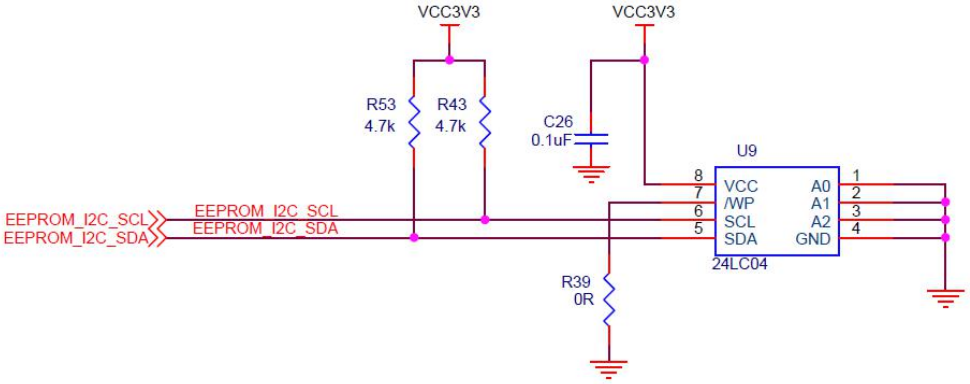


Figure 8-1: EEPROM Design

Figure 8-2 shows the EEPROM on AX516 board：

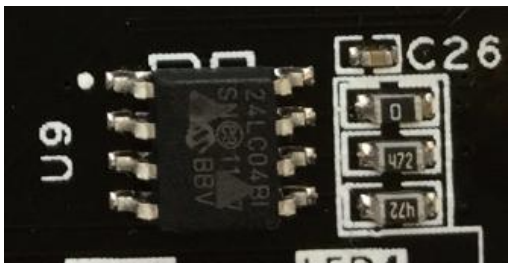


Figure 8-2: EEPROM on AX516 board

Table 8-1 detailed the EEPROM PIN assignment

Net Name	FPGA PIN
SDA	N5
SCL	P6

Table 8-1: EEPROM PIN Assignment

Part 9: Real time clock DS1302

The FPGA development board contains a real-time clock RTC chip, model DS1302. Its function is to provide the calendar function to 2099, with days, minutes, minutes, seconds and weeks. If time is required in the system, the RTC needs to be designed into the product. it need to connect a 32.768KHz

passive clock to provide an accurate clock source to the clock chip, so that the RTC can accurately provide clock information to the product. At the same time, in order to power off the product, the real-time clock can still run normally. Generally, a battery is required to supply power to the clock chip. In Figure 8.1, U7 is the battery holder. We put the button battery (model CR1220, voltage is 3V) into the battery. When the system is powered off, the button battery can also supply power to the DS1302, so that regardless of whether the product is powered or not, the DS1302 will operate normally without interruption and provide continuous time information. Figure 9-11 shows the schematic of the DS1302

The hardware design of RTC is showed as Figure 9-1:

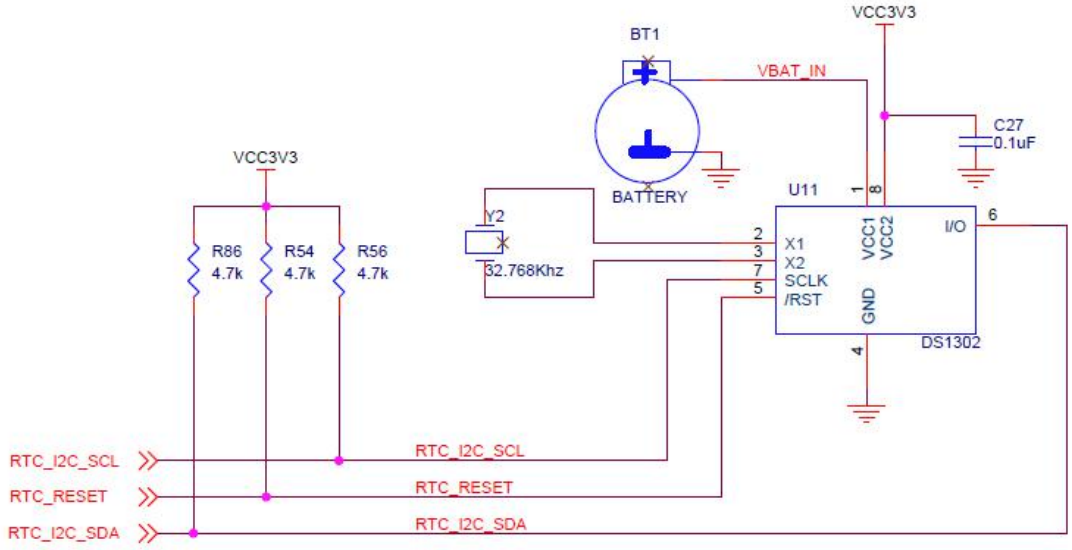


Figure 9-1: RTC Hardware Design

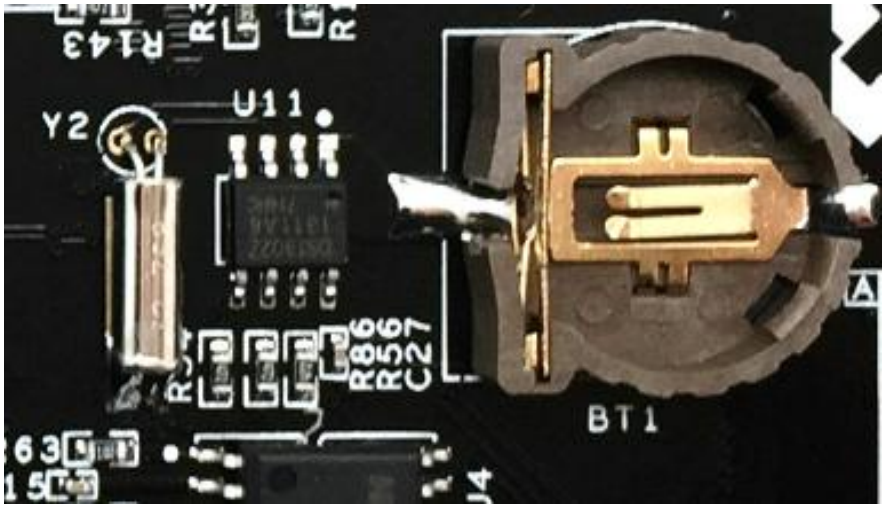


Figure 9-2: DS1302 Circuit Onboard

Table 9-1 detailed the DS1302 Pin Assignment：

Net Name	FPGA PIN
RTC_I2C_SCL	P16
RTC_RESET	T7
RTC_I2C_SDA	P15

Table 9-1: The DS1302 Pin Assignment

Part 10: Gigabit Ethernet Interface

The FPGA development board provides network communication services through the Realtek RTL8211EG Ethernet PHY chip. The RTL8211EG chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the GMII interface. RTL8211EG supports MDI/MDX adaptive, various speed adaptations, Master/Slave adaptation, and support for MDIO bus for PHY register management.

The RTL8211EG will detect the level status of some specific IOs to determine their working mode after powered on. Table 9-1 describes the default setup information after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
SELRGV	3.3V, 2.5V, 1.5/1.8V voltage selection	3.3V
AN[1:0]	Auto-negotiation configuration	(10/100/1000M) adaptive
RX Delay	RX clock 2ns delay	Delay
TX Delay	TX clock 2ns delay	Delay
Mode	RGMII or GMII selection	GMII

Table 10-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the GMII bus, the transmission clock is 125Mhz. The receive clock E_RXC is provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is sampled on the rising edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the MII bus, the transmission clock is 25Mhz. The receive clock E_RXC and transmit clock E_TXC are provided by the PHY chip, , and the data is sampled on the rising edge of the clock.

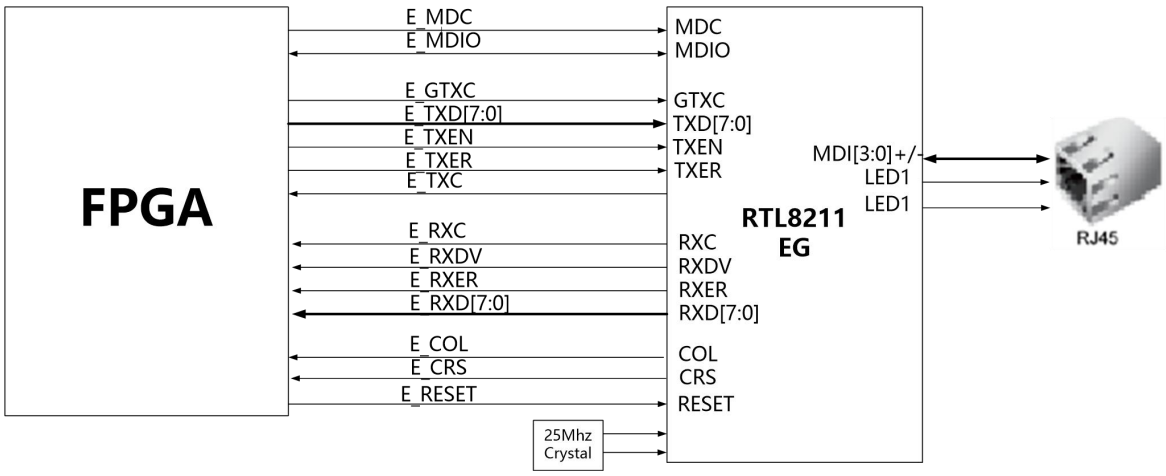


Figure 10-1: Gigabit Ethernet Interface Schematic

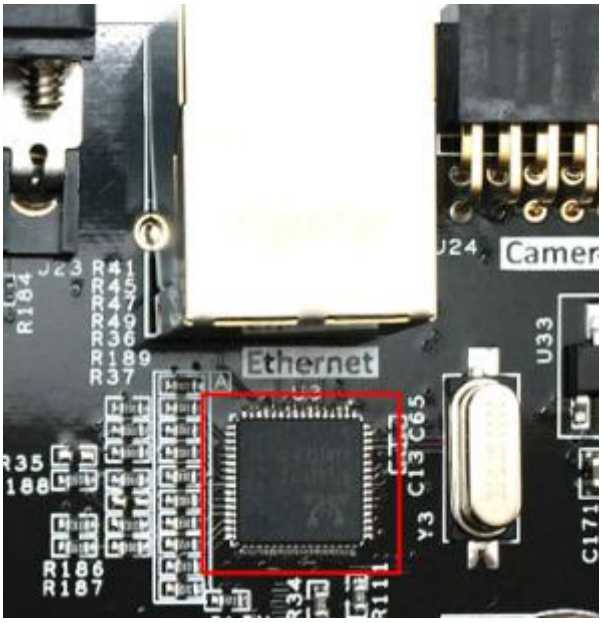


Figure 10-2: Gigabit Ethernet interface on the FPGA board

Ethernet pin assignments are as follows：

Signal Name	FPGA Pin	Description
E_GCLK	L15	Ethernet GMII transmit clock
E_TXD0	H16	Ethernet Transmit Data bit0
E_TXD1	G16	Ethernet Transmit Data bit1
E_TXD2	G18	Ethernet Transmit Data bit2
E_TXD3	J13	Ethernet Transmit Data bit3
E_TXD4	K14	Ethernet Transmit Data bit4
E_TXD5	L12	Ethernet Transmit Data bit5
E_TXD6	L13	Ethernet Transmit Data bit6
E_TXD7	K15	Ethernet Transmit Data bit7
E_TXEN	K17	Ethernet transmit enable signal
E_TXER	J18	Ethernet transmit error signal
E_TXC	K16	Ethernet MII transmit clock
E_RXC	L16	Ethernet GMII receive clock
E_RXDV	H15	Ethernet receive data valid signal
E_RXER	H14	Ethernet receive data error
E_RXD0	G13	Ethernet Receive Data Bit0

E_RXD1	E16	Ethernet Receive Data Bit1
E_RXD2	E18	Ethernet Receive Data Bit2
E_RXD3	K12	Ethernet Receive Data Bit3
E_RXD4	K13	Ethernet Receive Data Bit4
E_RXD5	F17	Ethernet Receive Data Bit5
E_RXD6	F18	Ethernet Receive Data Bit6
E_RXD7	H13	Ethernet Receive Data Bit7
E_COL	H12	Ethernet Collision signal
E_CRS	D18	Ethernet Carrier Sense Signal
E_RESET	J16	Ethernet Reset Signal
E_MDC	D17	Ethernet Management Clock
E_MDIO	G14	Ethernet Management Data

Part 11: USB to Serial Port

The FPGA development board contains the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface. It can be connected to the USB port of the PC for serial data communication by using a USB cable.

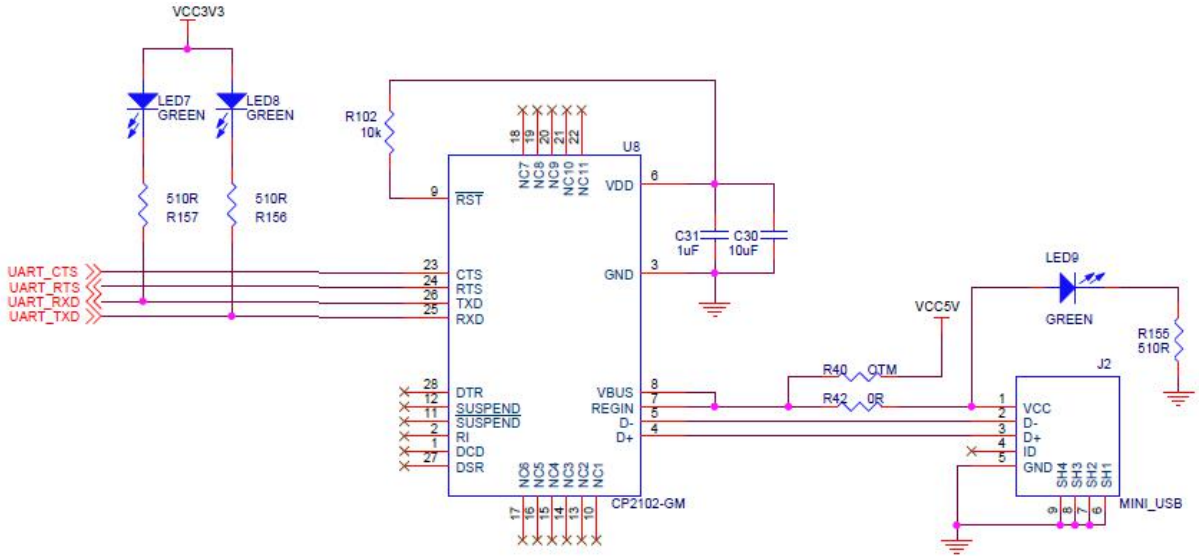


Figure 11-1: USB to Serial Port Interface

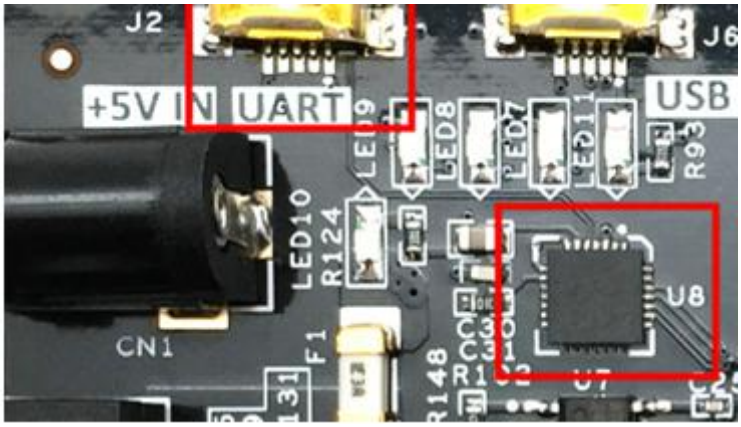


Figure 11-2: USB to Serial Port Circuit Onboard

At the same time, three LED indicators (LED7, LED8, LED9) are set for the serial port signal. When the UART port (J2) is connected to the USB port of the PC, LED9 is on; LED7 and LED8 will indicate whether the serial port has data or whether there is data acceptance.

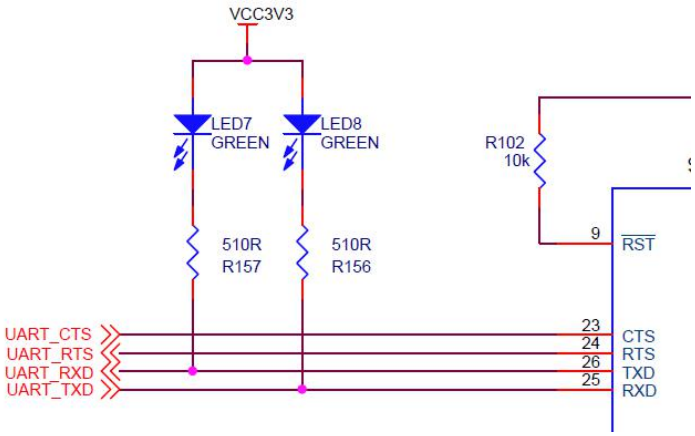


Figure 11-3: USB to serial signal indicator

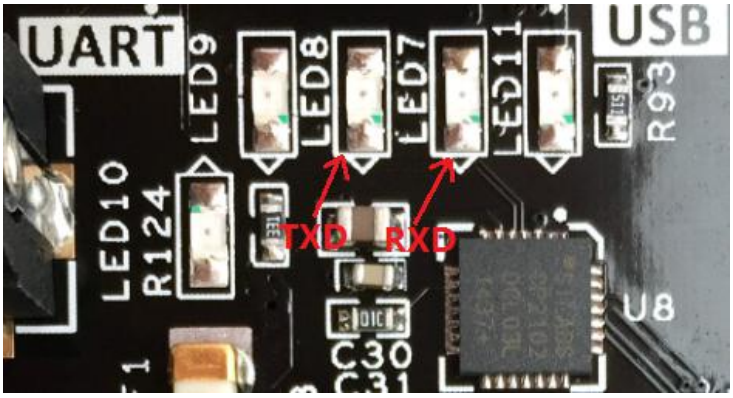


Figure 11-4: USB to serial signal indicator on FPGA Board

Serial port pin assignment:

Pin Name	FPGA Pin
UART_RXD	B2
UART_TXD	C4
UART_CTS	D6
UART_RTS	A2

Table11-1: The PIN Assignment of Serial Port

Part 12: VGA Port

VGA interface, I believe many friends will not be unfamiliar, because this interface is the most important interface on the computer monitor. From the era of huge CRT monitors, the VGA interface has been used, and it has been used until now, and the VGA interface is also called For the D-Sub interface.

The VGA connector is a D-type connector with a total of 15 pinholes divided into three rows of five. More important are the three RGB color component signals and the two scan sync signals HSYNC and VSYNC pins.

Pins 1, 2, and 3 are red, green, and blue primary color analog voltages, which are 0 to 0.714V peak-peak, 0V is colorless, and 0.714V is full color. Some non-standard displays use a full color level of 1Vpp.

The three primary color source terminals and terminal matching resistors are both 75 ohms, detailed as Figure 12-1

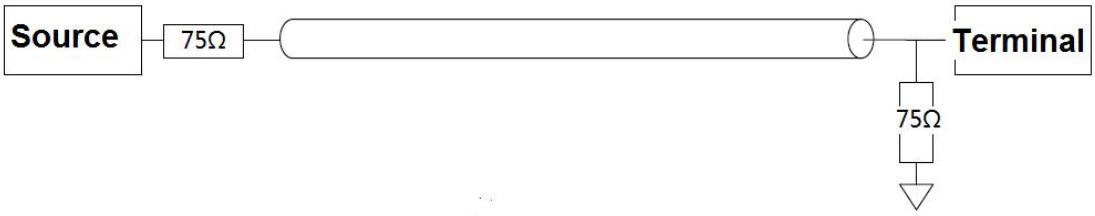


Figure 12-1: VGA video signal transmission diagram

HSYNC and VSYNC are line data synchronization and frame data synchronization, respectively, which are TTL levels. The FPGA can only output digital signals, while the R, G, and B required by VGA are analog signals. The digital to analog signal of VGA is realized by a simple resistor circuit. This resistor circuit can generate 32 gradient grade red and blue signals and 64 gradient grade green signals (RGB 5-6-5). Figure 12-2 detailed the VGA interface hardware design.

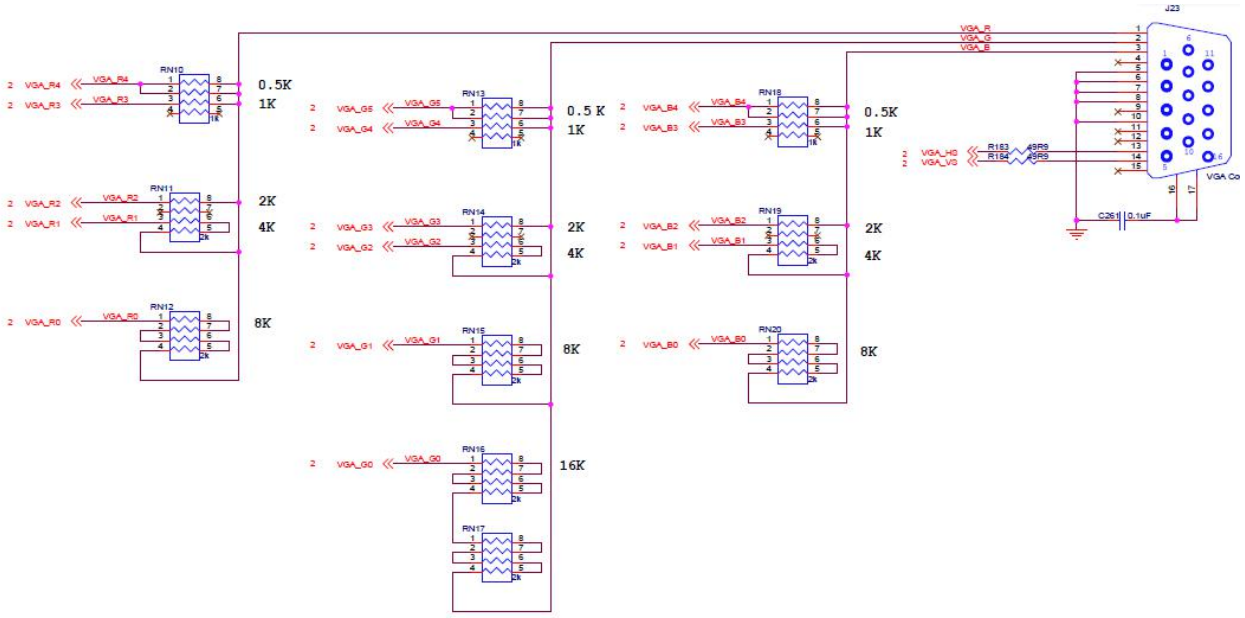


Figure 12-2: VGA Interface Hardware Design

Figure 12-3: VGA Interface on board

VGA Interface Pin Assignment

Signal Name	FPGA PIN	Description
VGA_B[0]	B14	BLUE[0]
VGA_B[1]	A16	BLUE[1]
VGA_B[2]	F16	BLUE[2]
VGA_B[3]	F15	BLUE[3]
VGA_B[4]	B16	BLUE[4]
VGA_G[0]	C14	GREEN[0]
VGA_G[1]	A15	GREEN[1]
VGA_G[2]	A12	GREEN[2]
VGA_G[3]	A13	GREEN[3]
VGA_G[4]	C15	GREEN[4]
VGA_G[5]	A14	GREEN[5]
VGA_R[0]	F13	RED[0]
VGA_R[1]	D14	RED[1]
VGA_R[2]	C13	RED[2]
VGA_R[3]	E13	RED[3]
VGA_R[4]	F14	RED[4]
VGA_HS	C17	Horizontal sync signal
VGA_VS	C18	Vertical sync signal

Table 12-1: The Pin Assignment of VGA Interface

Part 13: USB 2.0

The board uses Cypress CY7C68013A USB2.0 controller chip to realize

high-speed data communication between PC and FPGA. CY7C68013A controller fully complies with the universal serial bus protocol version 2.0 specifications, supports full speed (12Mbit/s) and low speed (480Mbit/s) mode. The user can perform USB2.0 data communication by connecting the USB port of the PC with the USB cable and the MINI type USB port (J6) of the development board.

The CY7C68013A is a microcontroller with integrated USB 2.0. It integrates a USB 2.0 transceiver, SIE (serial interface engine), enhanced 8051 microcontroller and programmable external interface into a single chip. The communication between CY7C68013A and other devices is very simple. It provides GPIF in FIFO mode for seamless data exchange with FPGA, DSP, ATA, UTOPIA, EPP, PCMCIA etc.

The CY7C68013A transceiver is clocked by a 24MHz crystal oscillator. Figure 13-1 detailed the FPGA and CY7C68013A connection.

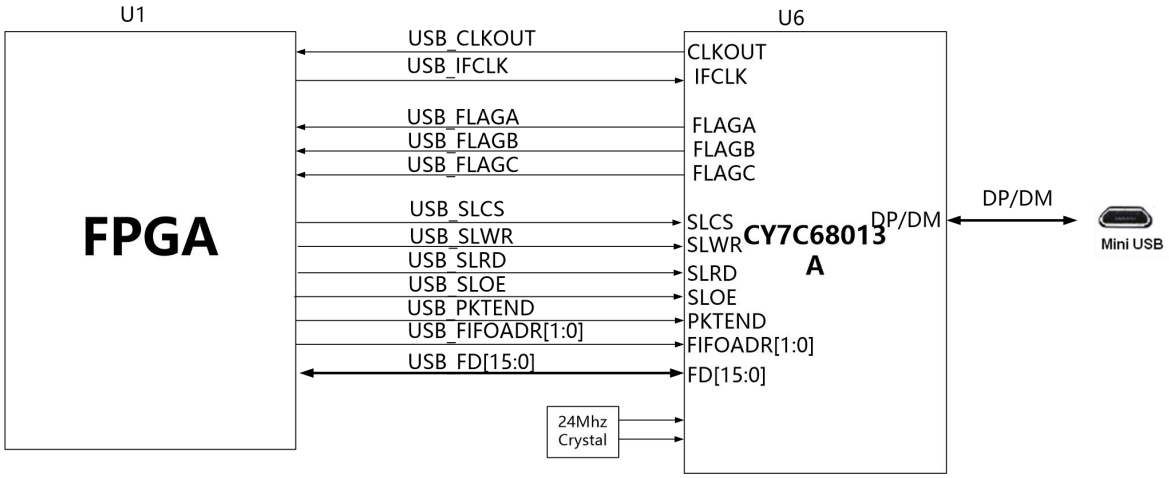


Figure 13-1: The FPGA and CY7C68013A connection

Figure 13-2 detailed the USB2.0 part circuit on board, U6 is CY7C68013A, J6 is USB interface

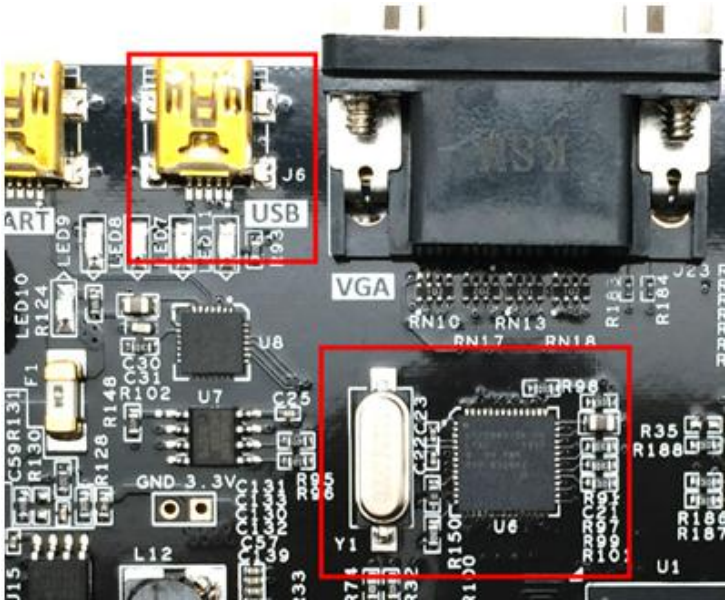


Figure 13-2: USB2.0 part circuit on board

USB 2.0 Pin Assignment

Pin Name	FPGA Pin	Description
USB_CLKOUT	C9	12-, 24- or 48 MHz clock output
USB_IFCLK	C6	Synchronous communication clock signal
USB_FLAGA	A6	Status output signal
USB_FLAGB	C7	Status output signal
USB_FLAGC	A7	Status output signal
USB_SLCS	B9	Slave FIFO chip selection
USB_SLWR	A5	Slave FIFO write signal
USB_SLRD	B6	Slave FIFO read signal
USB_SLOE	C8	Slave FIFO data output enable
USB_PKTEND	B8	Packet end signal
USB_FIFOADR[0]	A8	FIFO address 0
USB_FIFOADR[1]	A9	FIFO address 0
USB_FD[0]	A4	USB data Bit0
USB_FD[1]	D8	USB data Bit1
USB_FD[2]	B4	USB data Bit2
USB_FD[3]	G9	USB data Bit3

USB_FD[4]	A3	USB data Bit4
USB_FD[5]	F9	USB data Bit5
USB_FD[6]	C5	USB data Bit6
USB_FD[7]	B3	USB data Bit7
USB_FD[8]	A10	USB data Bit8
USB_FD[9]	D11	USB data Bit9
USB_FD[10]	C11	USB data Bit10
USB_FD[11]	C10	USB data Bit11
USB_FD[12]	D9	USB data Bit12
USB_FD[13]	B11	USB data Bit13
USB_FD[14]	A11	USB data Bit14
USB_FD[15]	B12	USB data Bit15

Part 14: SD card slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted substantial research and development. In 2000, these companies initiated the establishment of the SD Association (Secure Digital Association, SDA), which has a strong lineup and attracted a large number of manufacturers. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

SD card is a very popular storage device now. The extended SD card supports SPI mode and SD mode. The SD card used is a MicroSD card. The hardware design of SD socket is showed as Figure 14-1.

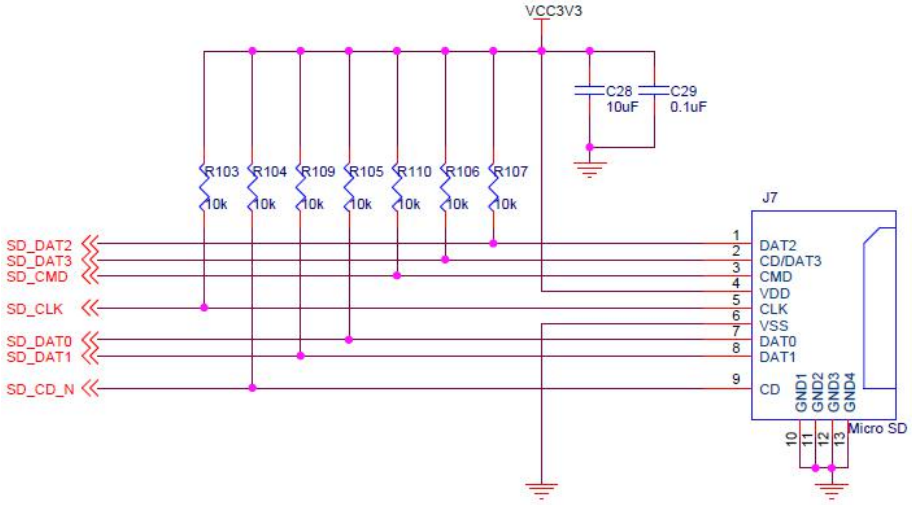


Figure 14-1: SD Socket Design

Figure 14-2: SD Card Slot On board

SD Card Slot Pin Assignment:

SD Mode	
Pin Name	FPGA Pin
SD_CLK	U18
SD_CMD	P15
SD_CD_N	M13
SD_DAT0	N14
SD_DAT1	M14
SD_DAT2	P16
SD_DAT3	L14

Table 14-1: The Pin Assignment of SD Card Slot

Part 15: Expansion Header

The development board reserves 1 expansion ports, and the expansion port has 40 signals, of which 5V power supply 1 way, 3.3V power supply 2 way, ground 3 way, IO port 34 way. These IO ports are independent IO ports and are not multiplexed with other devices. The IO port is connected to Bank2 of the FPGA. The default level is 3.3V. It can be changed to 2.5V by adjusting the 0 ohm resistor on the board (R158 is not installed, when R159 is installed). Do not connect directly to a 5V device to avoid burning the FPGA. If you want to connect a 5V device, you need to connect a level shifting chip.

The FPGA IO pins on the expansion headers are connected to a 33ohm resistor for protection against high or low voltage level. The circuit of the expansion port (J3) is shown in Figure 15-1.

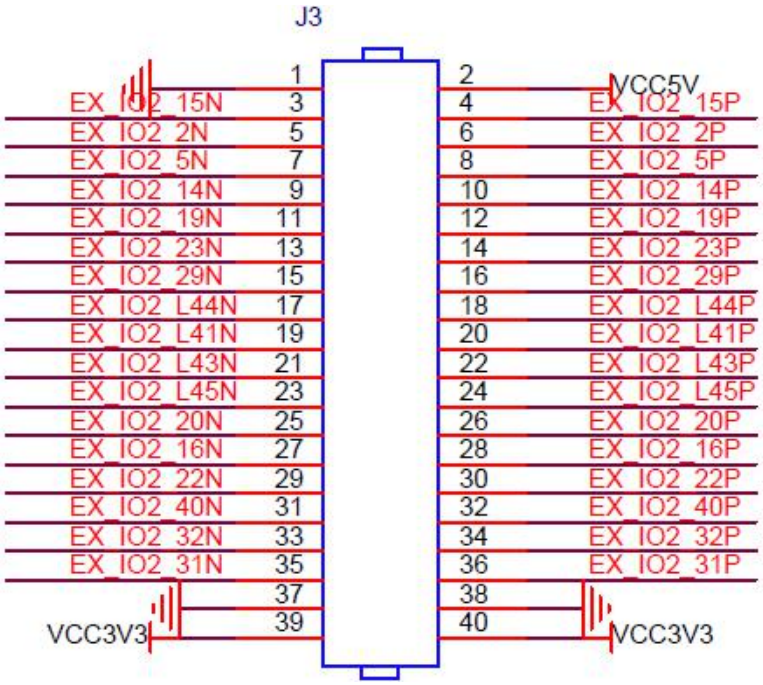


Figure 15-1: J3 Expansion Headers

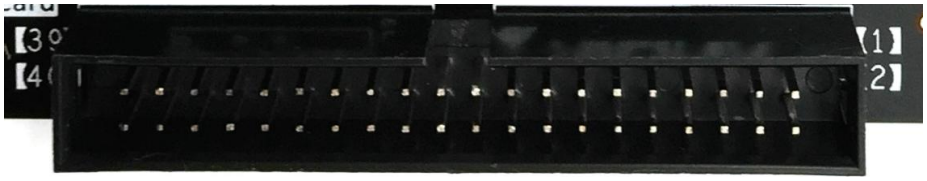


Figure 15-2: J3 Expansion Headers on Board

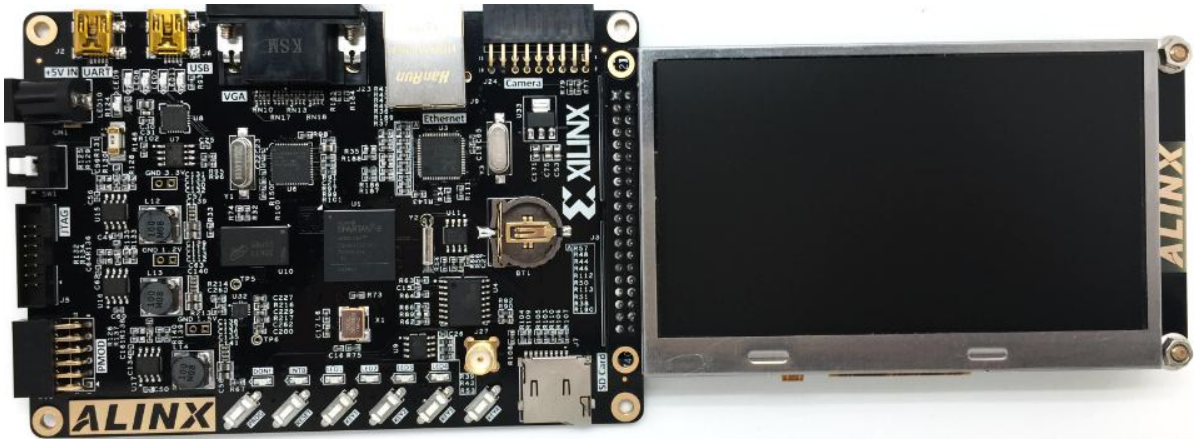


Figure 15-3: Expansion port connected the expansion module

J3 Expansion Port Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
1	GND	**2**	VCC5V
3	N11	**4**	M11
5	V16	**6**	U16
7	V15	**8**	U15
9	V13	**10**	U13
11	V12	**12**	T12
13	V11	**14**	U11
15	T10	**16**	R10
17	P8	**18**	N7
19	V8	**20**	U8
21	V7	**22**	U7
23	V6	**24**	T6
25	P11	**26**	N10
27	T11	**28**	R11

29	N9	**30**	M10
31	N8	**32**	M8
33	V9	**34**	T9
35	T8	**36**	R8
37	GND	**38**	GND
39	VCC3V3	**40**	VCC3V3

Part 16: LED

The FPGA development board contains six LEDs, including four user LEDs, two FPGA configuration LEDs. The schematic of the four user LEDs is shown in Figure 16-1. When the pin output of the FPGA is logic 0, the LED will be lit.

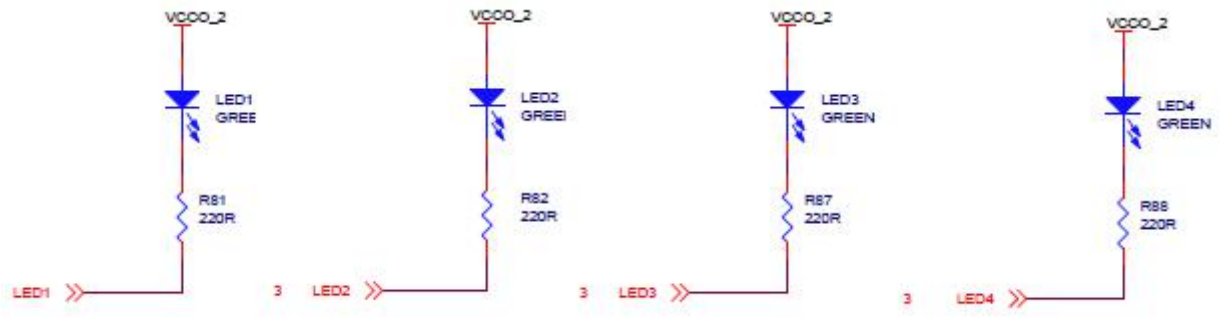


Figure 16-1: User LED schematic

The two FPGA configuration indicator LEDs are INIT LED and DONE LED respectively. When the FPGA has no configuration program, the INIT LED is lit and the DONE LED is off. After the FPGA configuration is successful, the INIT LED is off and the DONE LED is lit. The schematic diagram of the configuration indicator LED is shown in Figure 16-2

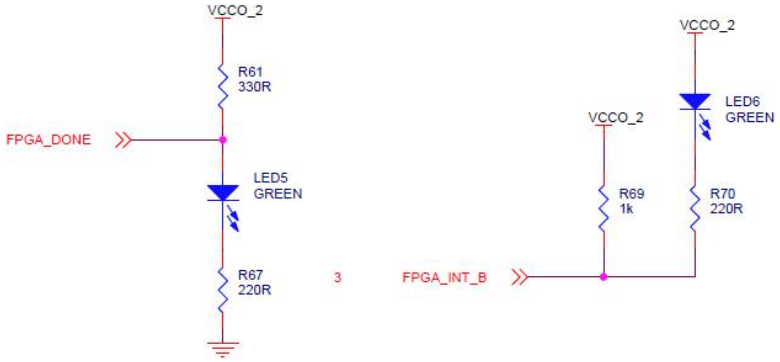


Figure 16-2: Configuration Indicator LED schematic

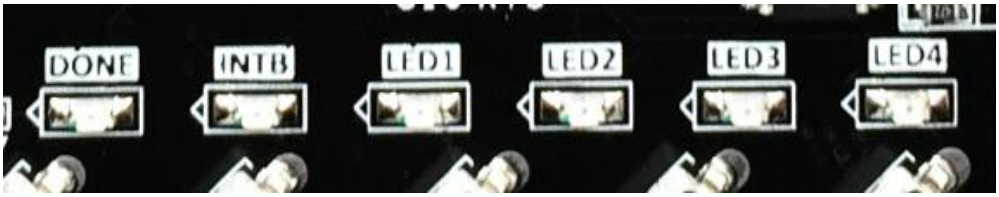


Figure 16-3: LEDs on Board

LEDs Pin Assignment

Pin Name	FPGA Pin
LED0	V5
LED1	R3
LED2	T3
LED3	T4

Table 16-1: The Pin Assignment of LEDs

Part 17: Buttons

The board has six buttons, it includes four user buttons (KEY1~KEY4) and two function buttons (PROG and RESET), **these six buttons are active low**. The hardware design of the four user keys is shown in Figure 17-1

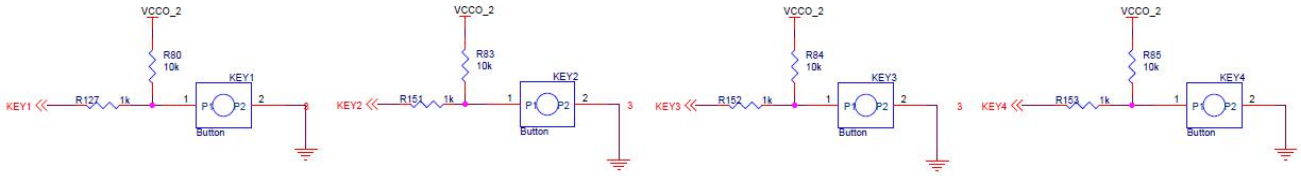


Figure 17-1: 4 user button schematics

The schematic diagram of the two function buttons is shown in Figure 16.2, where the Reset button is connected to the FPGA's normal IO for FPGA program reset, and the PROG button is connected to the FPGA's dedicated PROGRAM_B pin for FPGA program reconfiguration.

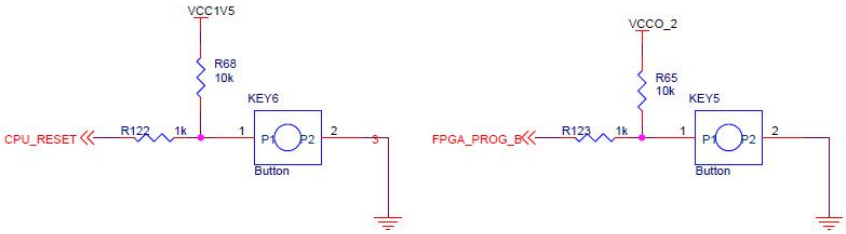


Figure 17-2: Two function buttons schematic

Figure 17-3: Six Buttons on Board

Buttons Pin Assignments

Button Name	FPGA Pin	Button Number
KEY1	P7	KEY 1
KEY2	R5	KEY 2
KEY3	T5	KEY 3
KEY4	U5	KEY 4
RESET	N4	KEY6
PROG	V2	KEY5

Part 18: Camera Module Interface

The AX516 FPGA development board includes an 18-pin CMOS camera interface that can be connected to the OV7670 camera module and the OV5640 camera module to enable video capture. After acquisition, the display can be connected via a TFT LCD module or a VGA interface. OV7670, 30W pixels, output resolution is 640*480; OV5640, 500W pixels, output resolution up to 2592 * 1944. Regarding camera selection, users can purchase according to their actual needs. The CMOS camera interface is designed as Figure 18-1:

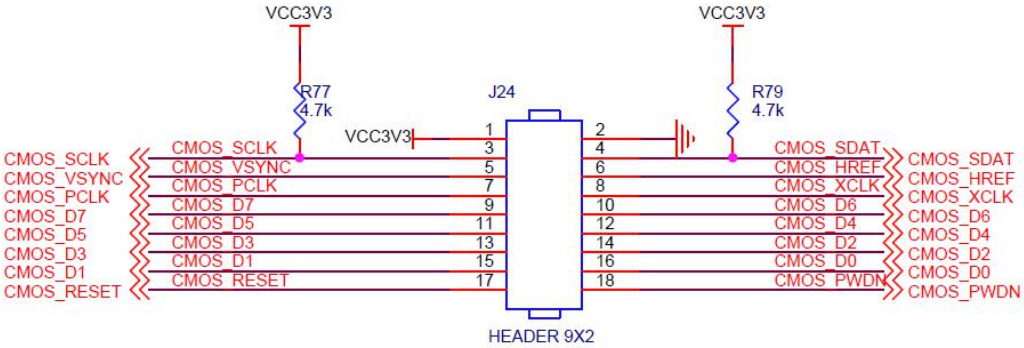


Figure 18-1: CMOS Camera interface

The Camera interface is showed as Figure 17-2 (Camera Module is required be purchase separately）

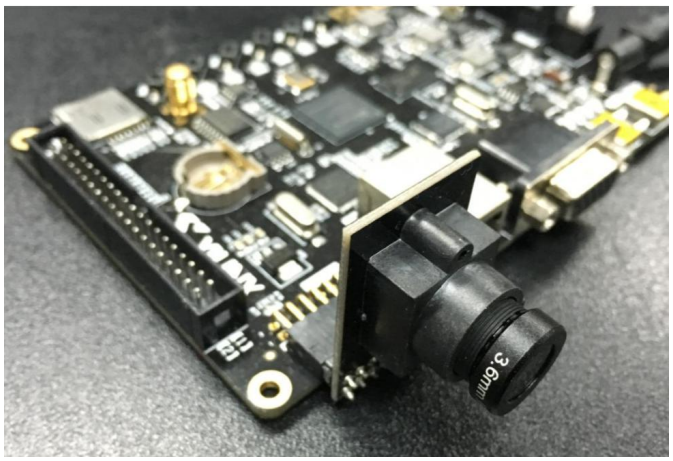


Figure 18-2: Camera Interface with OV5640 Camera Module

Camera interface pin assignment

Pin Name	FPGA Pin
CMOS_SCLK	T17
CMOS_SDAT	N16
CMOS_VSYNC	U17
CMOS_HREF	T18
CMOS_PCLK	H18
CMOS_XCLK	H17
CMOS_D[7]	P18
CMOS_D[6]	N15
CMOS_D[5]	N18
CMOS_D[4]	P17
CMOS_D[3]	M18
CMOS_D[2]	N17
CMOS_D[1]	L18
CMOS_D[0]	M16
CMOS_RESET	K18
CMOS_PWDN	L17

Table 18-1: The Pin Assignment of Camera Interface

Part 19: PMOD interface (AX516 Reserved)

The development board reserves a 12-pin 2.54mm pitch PMOD interface (J10) for connecting external modules or circuits. The PMOD interface is reserved for the AX516 development board (Spartan6 XC6SLX16 chip). However, for the AX545 development board, the pins of this PMOD interface are NC on the XC6SLX45 chip. These pins require special attention when the user is using it.

The PMOD interface pin is connected to the FPGA pin through a series 33 ohm resistor to protect the IO of the FPGA, so as to avoid damage to the FPGA caused by excessive external voltage or high current. The interface schematic

is shown in Figure 19-1

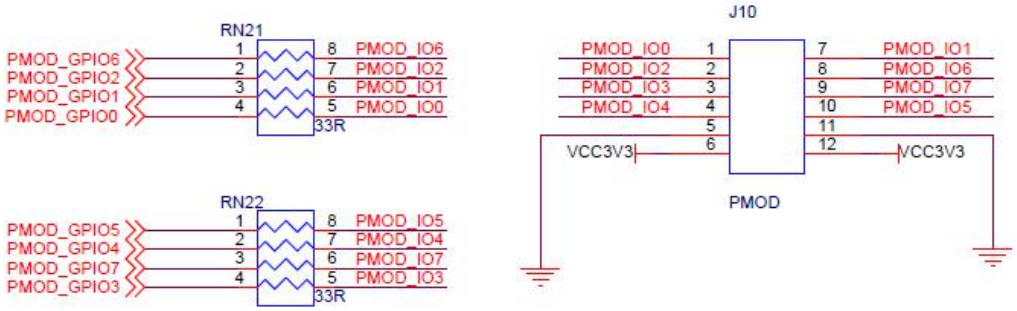


Figure 19-1: PMOD Interface Schematic

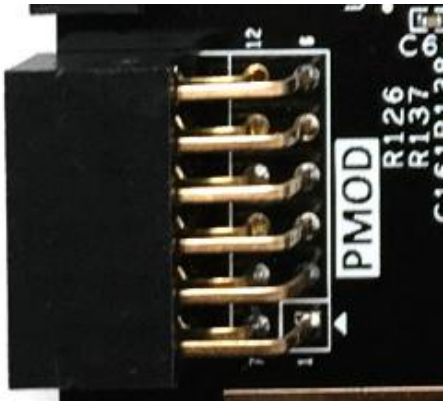


Figure 19-2: PMOD on FPGA Board

PMOD interface pin assignment

PMOD Pin	FPGA Pin	Description
1	G11	AX545 is not available
2	F11	AX545 is not available
3	E11	AX545 is not available
4	D12	AX545 is not available
5	GND	
6	VCC3V3	
7	F10	AX545 is not available
8	F12	AX545 is not available
9	E12	AX545 is not available

10	C12	AX545 is not available
11	GND	
12	VCC3V3	

Part 20: SMA Interface

The SMA interface (J27) on the development board is connected to the global clock input and output pins of the FPGA, and the user can freely use it according to his own needs. If the user needs to provide the input clock to the FPGA externally, the input voltage should not exceed +3.3V, otherwise the FPGA may be damaged. The SMA interface can also output the clock or PWM signal from the FPGA to the external device. The schematic diagram of the SMA interface is shown in Figure 20-1:

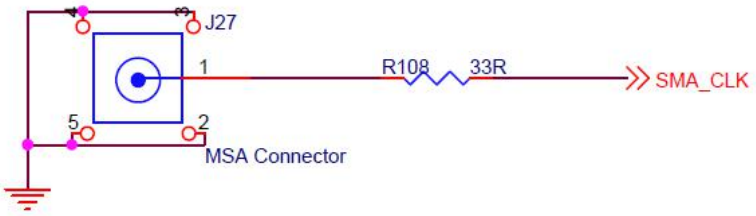


Figure 20-1: SMA clock interface schematic

Figure 20-2: SMA interface on board

SAM Interface Pin Assignment:

Pin Name	FPGA Pin
SMA_CLK	U10