

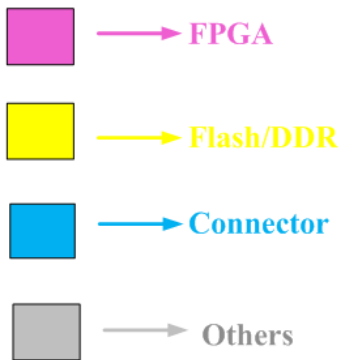
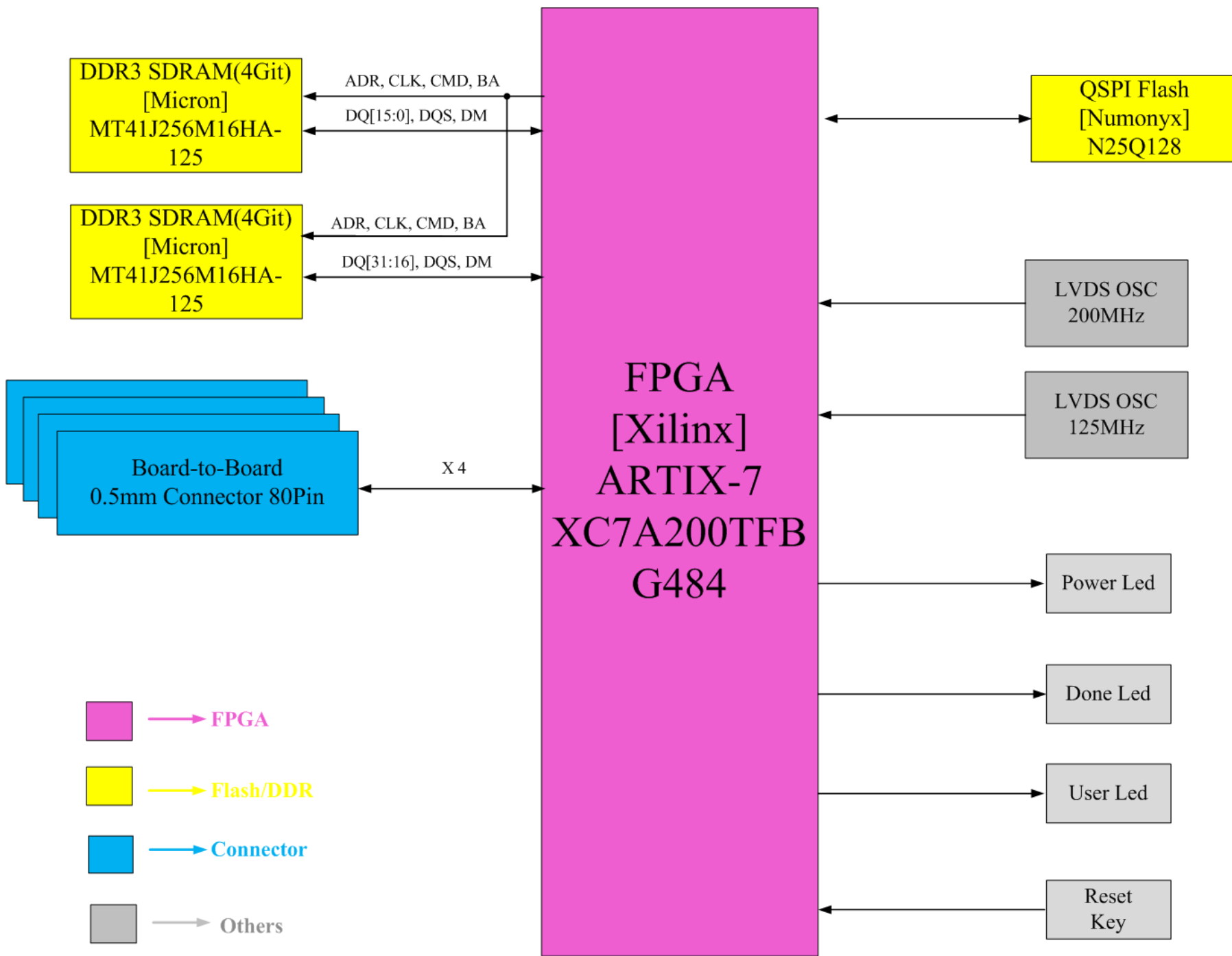
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| V1.0 | First Release | 2018-3-06 |
| | | |
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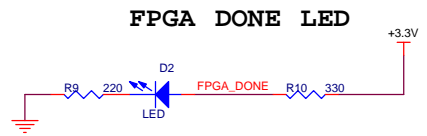
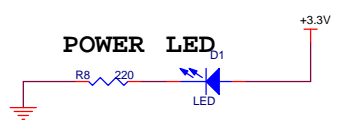
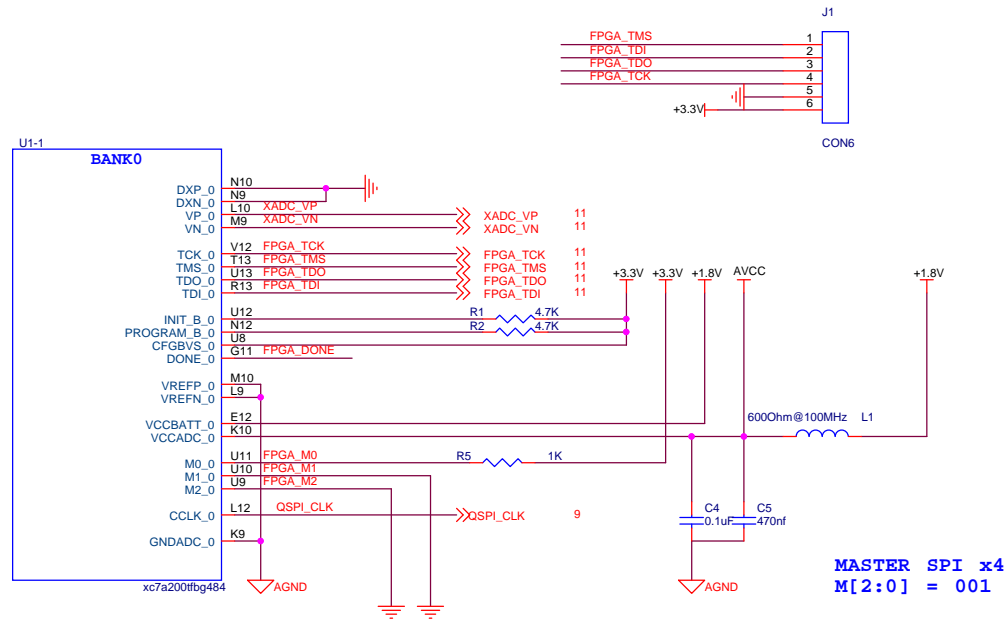
FPGA 核 心板

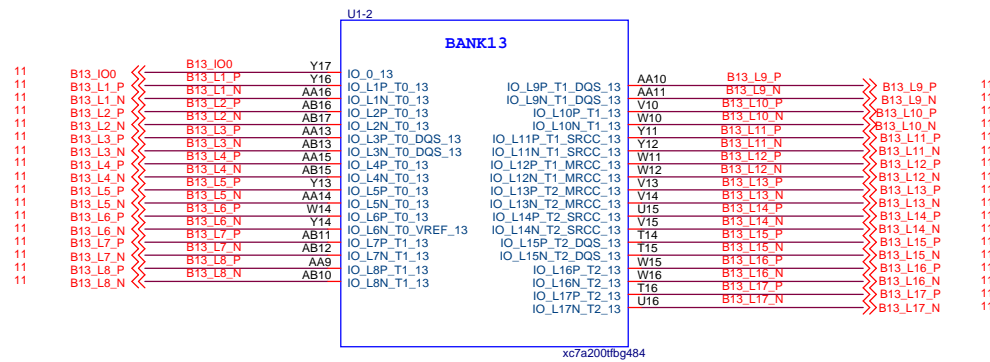
AC7200 Schematics

| Page Number | Description |
|-------------|----------------|
| Page01 | Cover Page |
| Page02 | Block Diagram |
| Page03 | FPGA BANK0 |
| Page04 | FPGA BANK13/14 |
| Page05 | FPGA BANK15/16 |
| Page06 | FPGA BANK34/35 |
| Page07 | FPGA BAN216 |
| Page08 | FPGA Power |
| Page09 | DDR3 |
| Page10 | CLOCK&FLASH |
| Page11 | POWER |
| Page12 | Connector |

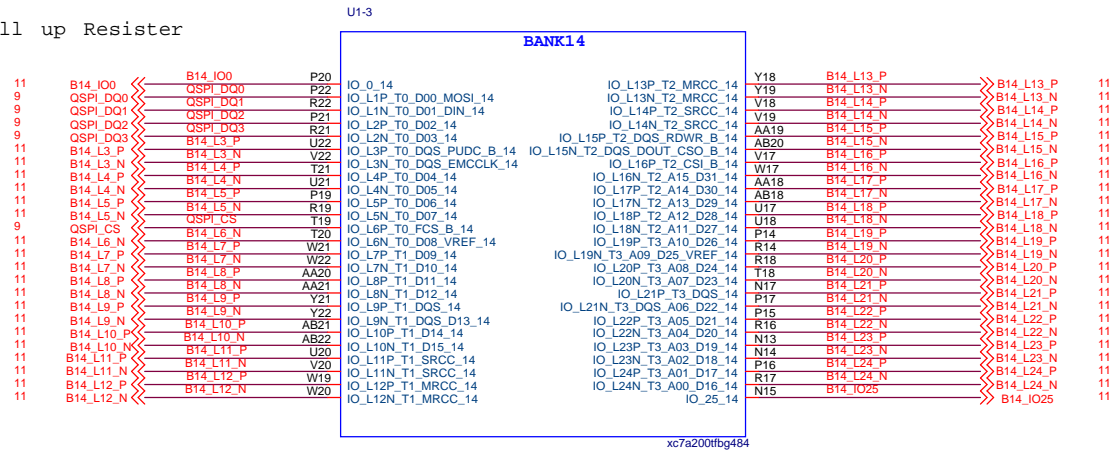
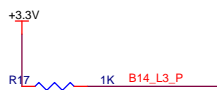
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| ALINX | | |
| Title Cover Page | | |
| Size | Document Number AC7200核心板 Schematics | Rev 1.0 |
| Date: | Friday, July 29, 2022 | Sheet 1 of 12 |

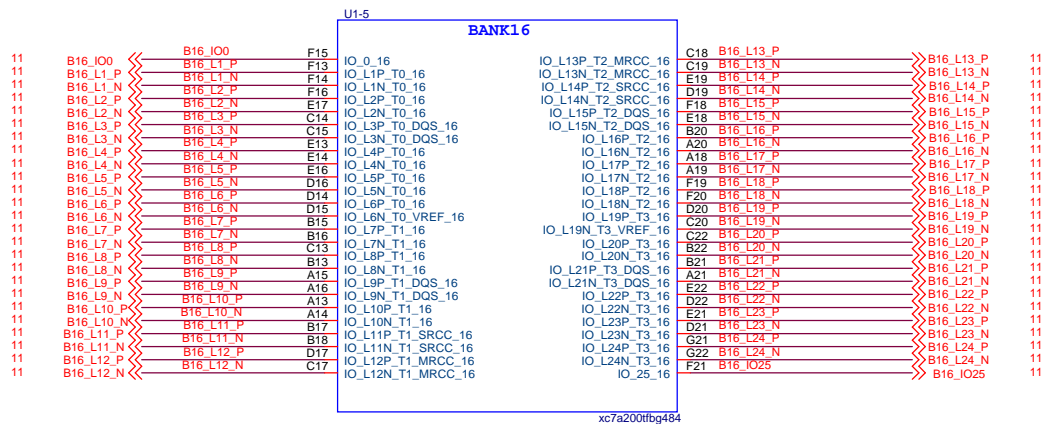
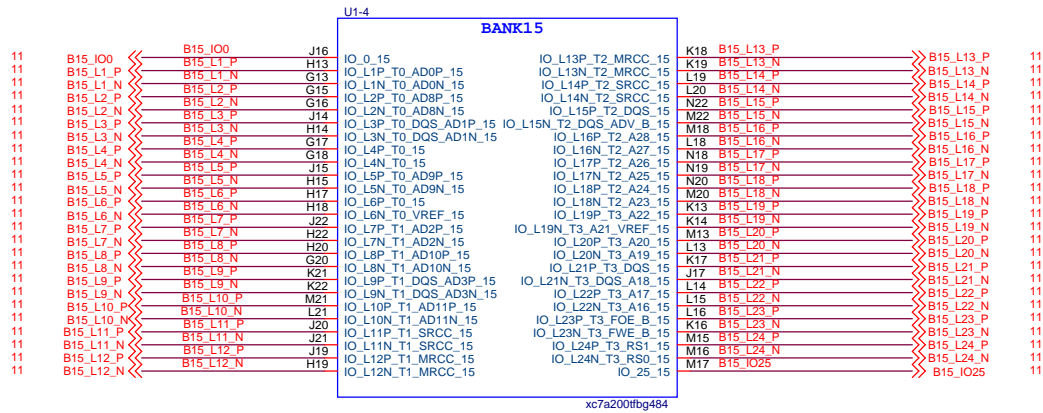


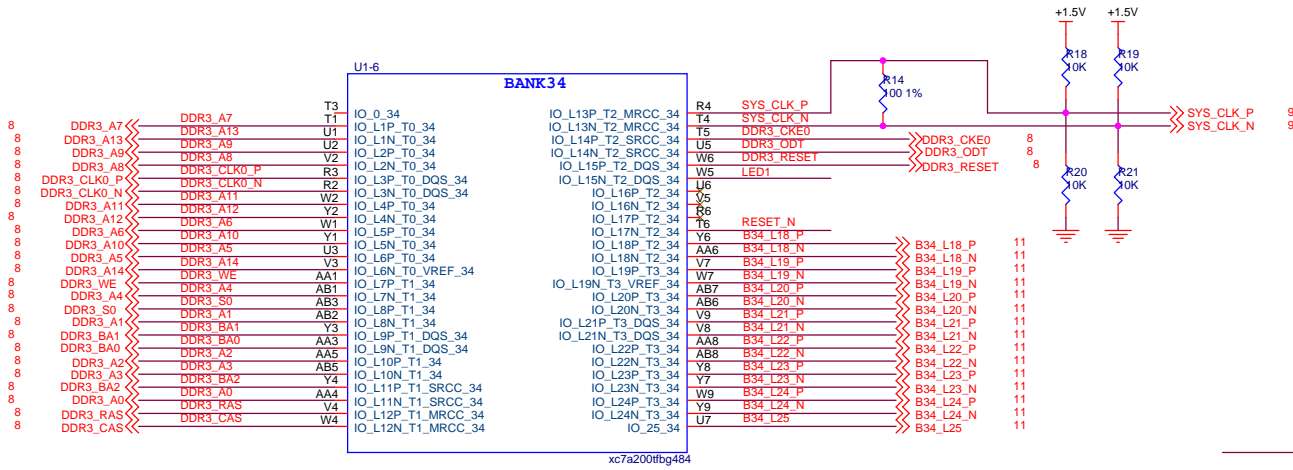




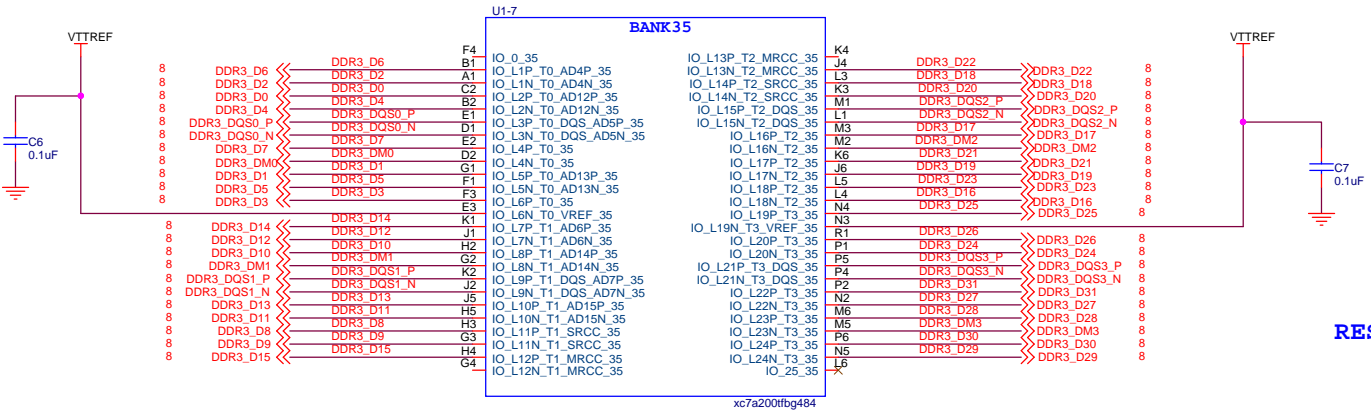
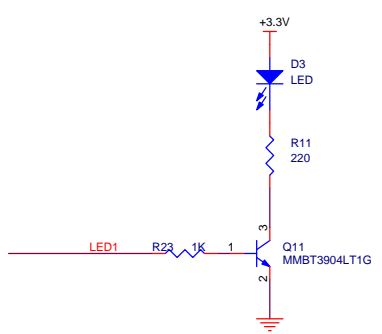
PUDC_B=1: Deactive internal Pull up Resister



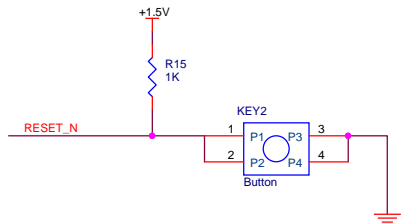




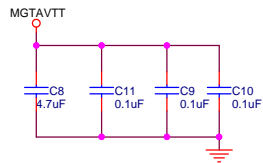
USER LED



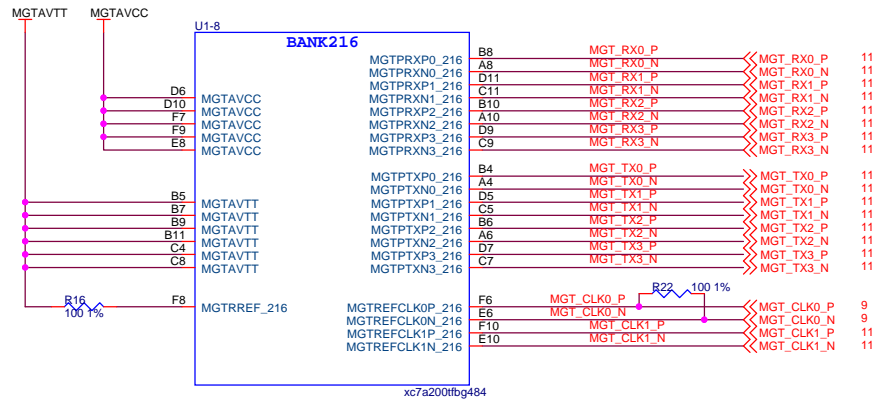
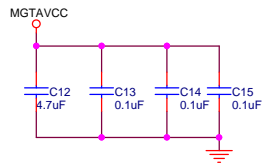
RESET KEY

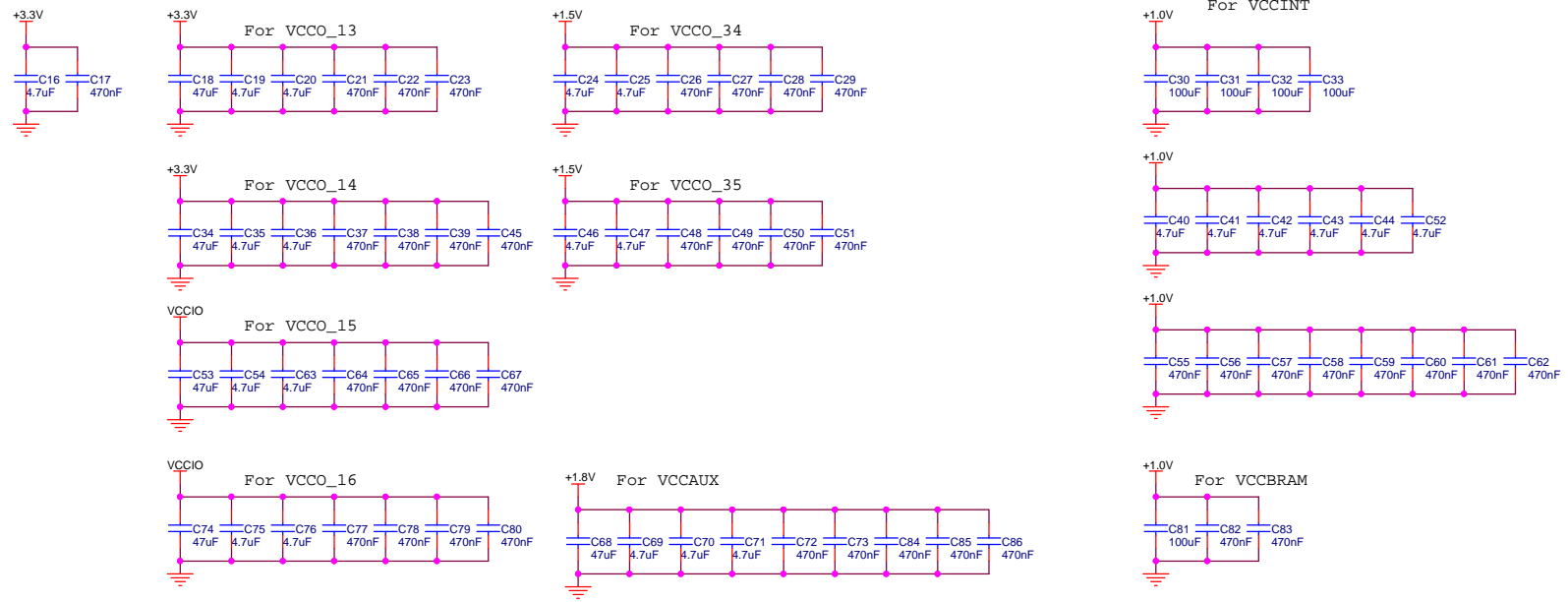
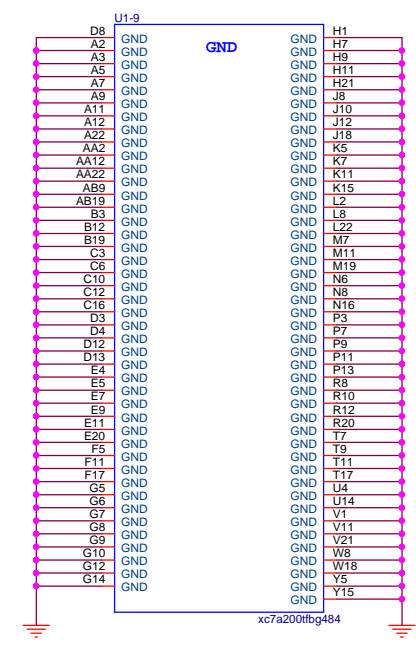
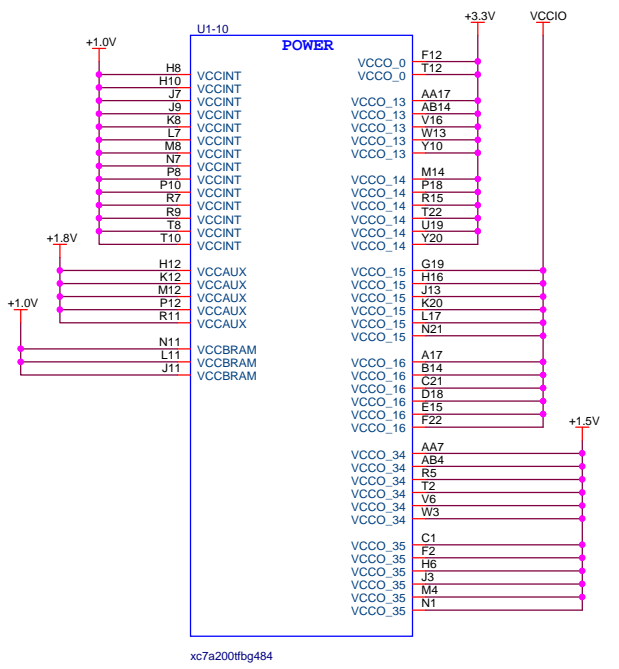


MGTAVTT 4.7uF(1) 0.1uF(2)



MGTAVCC 4.7uF(1) 0.1uF(2)



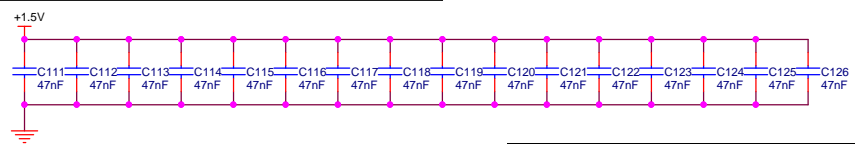
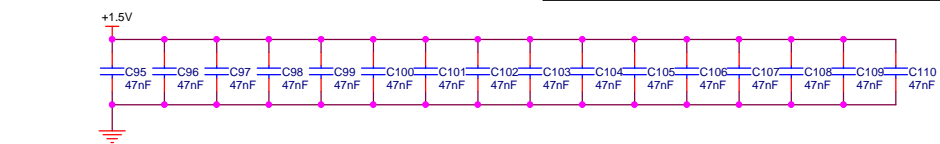
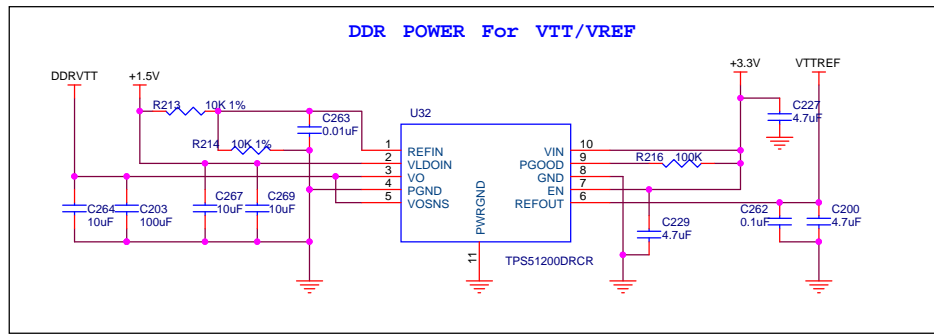
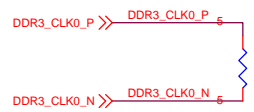
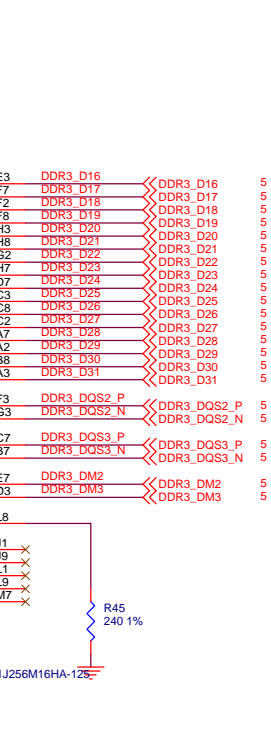
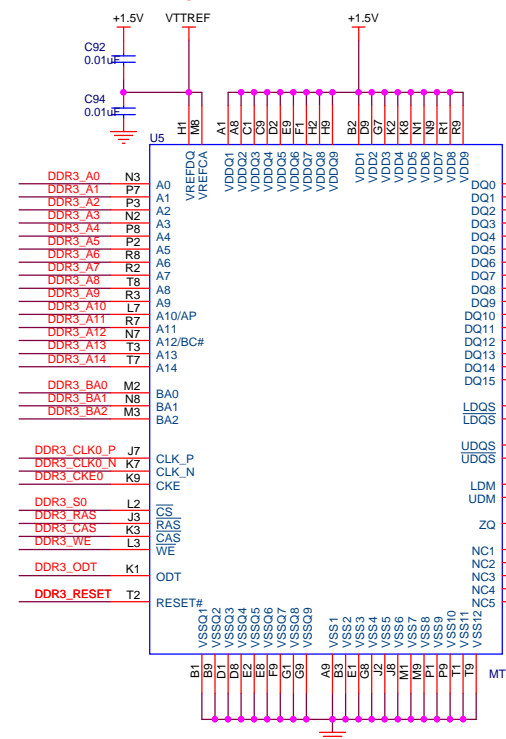
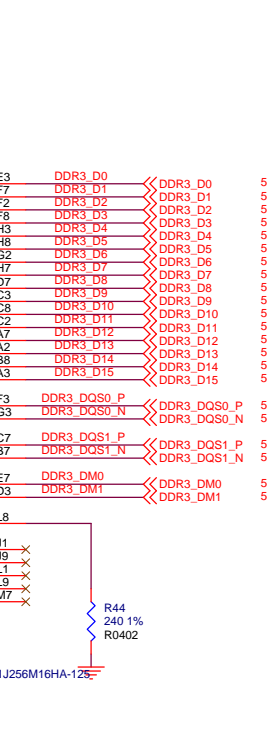
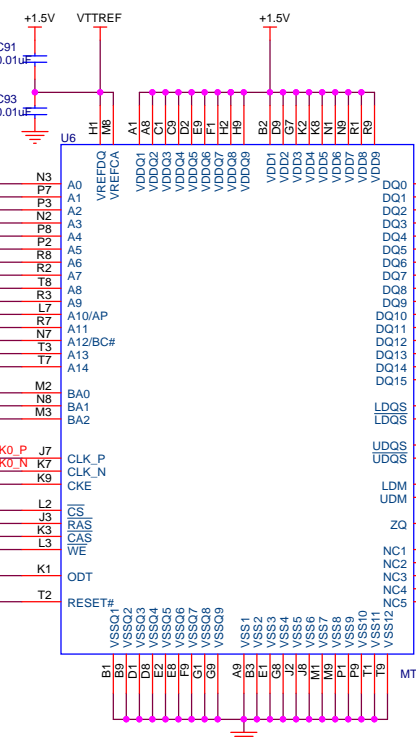
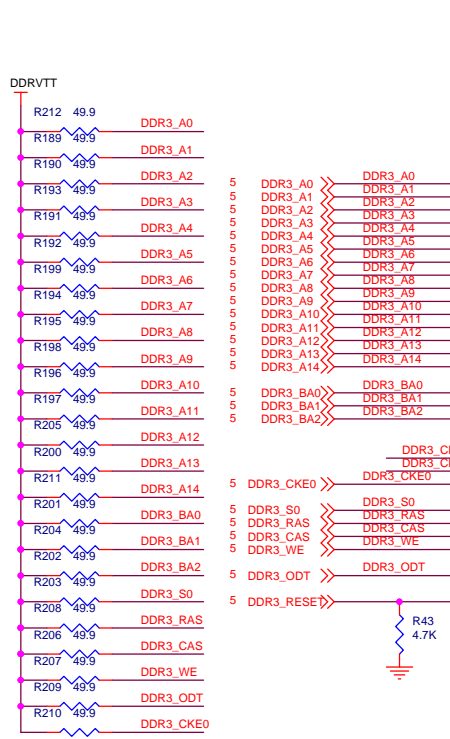
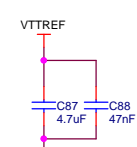
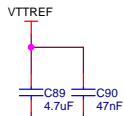
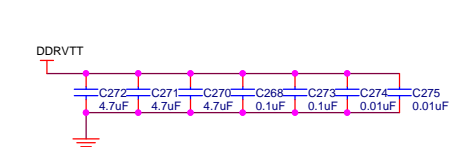


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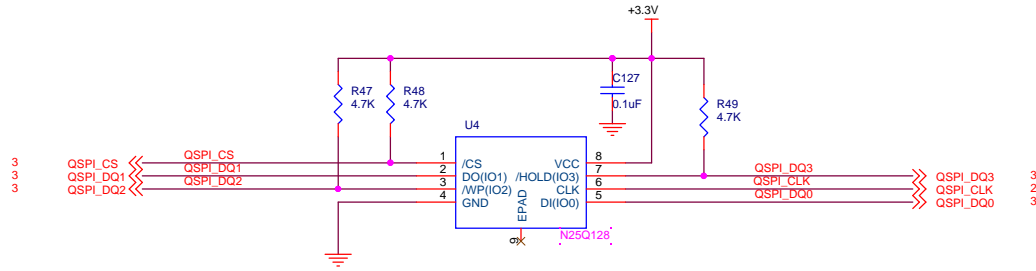
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Size: Document Number: **AC7200核心板 Schematics** Rev: 1.0

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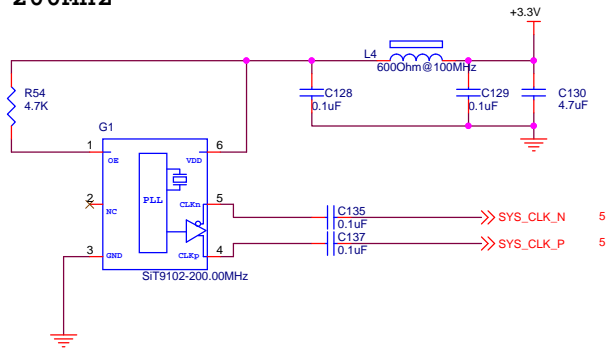


FPGA CONFIG SPI



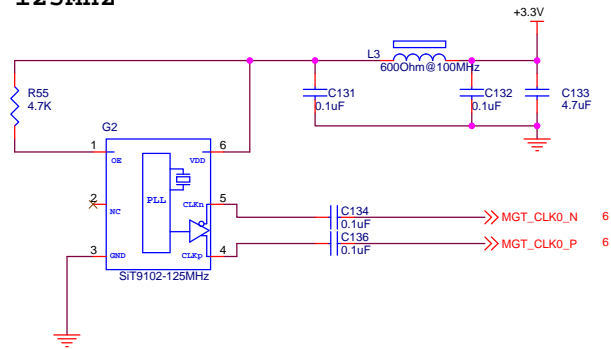
SYSTEM CLOCK

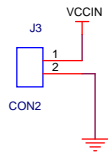
200MHz



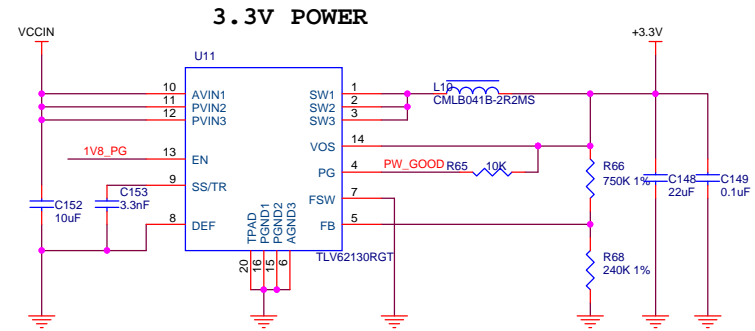
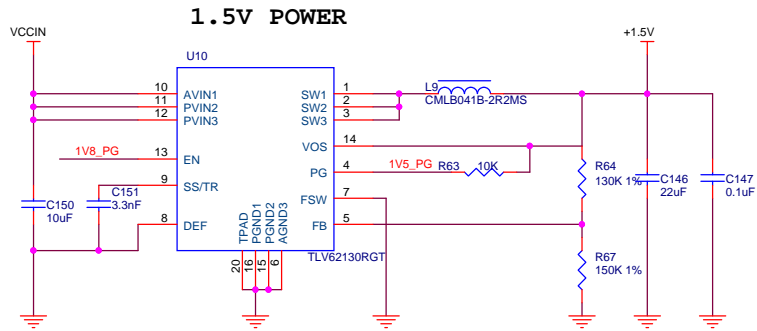
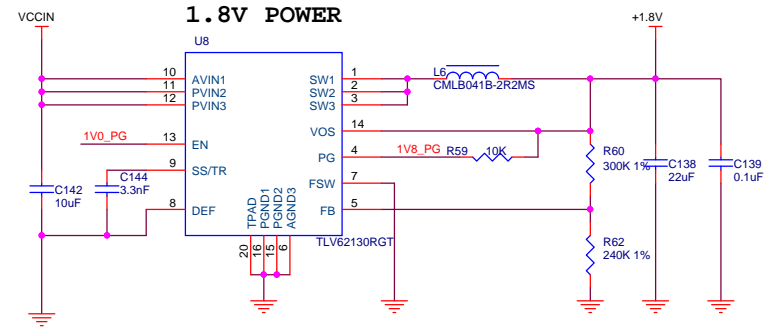
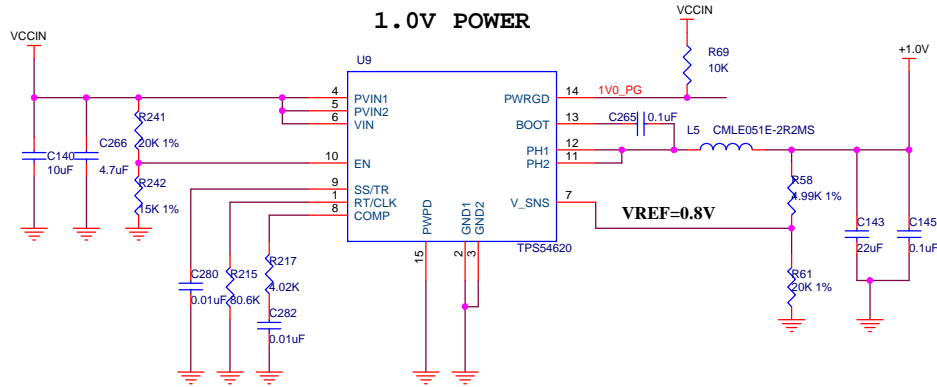
GTP CLOCK

125MHz





POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)->VCCO(1.5V and 3.3V)



POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)

