Spartan-7 FPGA Core Board

AC7050B

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.1	2019-04-25	Rachel Zhou	First Release

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Part 1: AC7050B core board

Part 1.1: AC7050B Core Board Introduction

AC7050B (core board model, the same below) FPGA core board, it is based on XILINX's Spartan 7 series XC7S50FGGA484. It is a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for high-speed data communication, video image processing, high-speed data acquisition, etc.

This AC7050B core board uses two pieces of MICRON's MT41J256M16HA-125 DDR3 chip, each DDR has a capacity of 4Gbit; two DDR chips are combined into a 32-bit data bus width, data clock frequency up to 333.3Mhz, such a configuration can meet the needs of high bandwidth data processing. The model of the 128Mb QSPI FLASH chip on the board is N25Q128, which is used to store the boot image file of the FPGA system

The AC7050B core board expands 114 standard IO ports of 3.3V level, of which 65 IOs can change the level standard by modifying the LDO chip on the core board. For users who need a lot of IO, this core board will be a good choice. Moreover, the routing between the FPGA chip and the interface is equal length and differential processing, and the core board size is only 45*55 (mm), which is very suitable for secondary development.

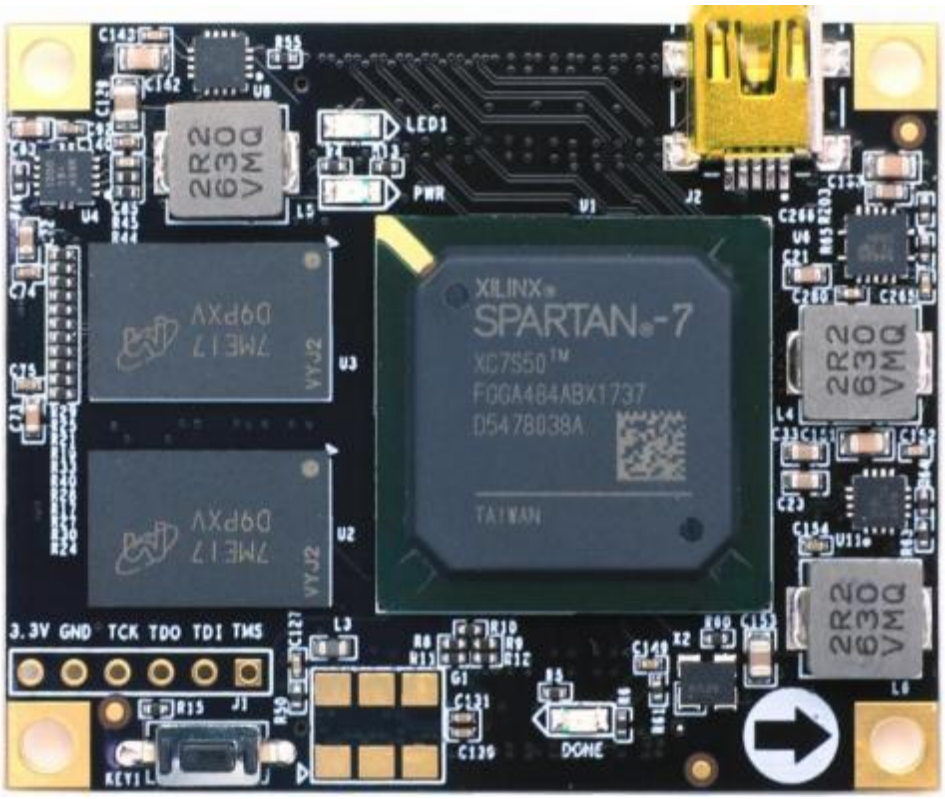

Figure 2-1-1: AC7050B Core Board (Front View)

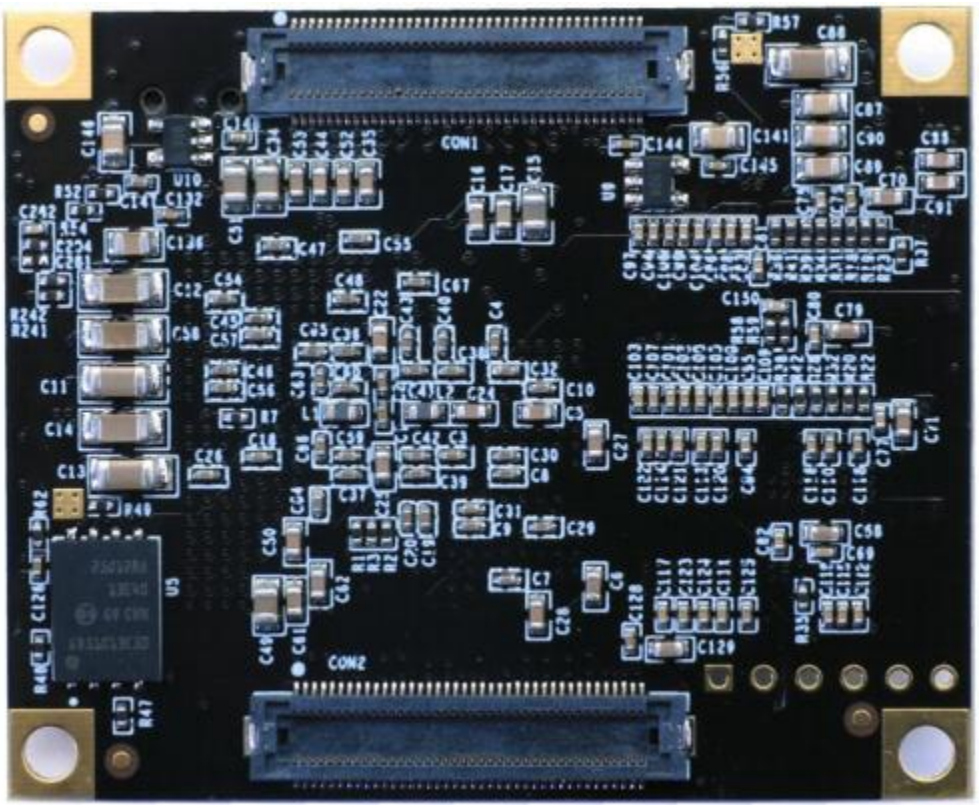

Figure 2-1-2: AC7050B Core Board (Rear View)

Part 1.2: FPGA Chip

As mentioned above, the FPGA model we use is **XC7S50FGGA484**, which belongs to Xilinx's Spartan7 series. The speed grade is 1, and the temperature grade is commercial grade. This model is a FGGA484 package with 484 pins. Xilinx Spartan7 FPGA chip naming rules as below

Figure 2-2-1: The Specific Chip Model Definition of Spartan7 Series

Figure 2-2-2: FPGA chip on board

The main parameters of the FPGA chip XC7S50 are as follows

		I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V, 0.95V)					
	Part Number	XC7S6	XC7S15	XC7S25	XC7S50	XC7S75	XC7S100
Logic Resources	Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
	Slices	938	2,000	3,650	8,150	12,000	16,000
	CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	10	45	75	90	120
	Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
I/O Resources	Max. Single-Ended I/O Pins	100	100	150	250	400	400
	Max. Differential I/O Pairs	48	48	72	120	192	192
Embedded Hard IP Resources	DSP Slices	10	20	80	120	140	160
	Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
	Configuration AES / HMAC Blocks	0	0	1	1	1	1
Speed Grades	Commercial Temp (C)	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
	Industrial Temp (I)	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L
	Expanded Temp (Q)	-1	-1	-1	-1	-1	-1
	Package[1]	Body Area (mm)	Available User I/O: 3.3V SelectIO™ HR I/O				
	CPGA196	8x8	100	100			
	CSGA225	13x13	100	100	150		
	CSGA324	15x15			150	210	
	FTGB196	15x15	100	100	100	100	
	FGGA484	23x23				250	338	338
	FGGA676	27x27					400	400

FPGA power supply system

XILINX Spartan7 FPGA power supplies are V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCIO}. V_{CCINT} is the FPGA core power supply pin, which needs to be connected to 1.0V; V_{CCBRAM} is the power supply pin of FPGA block RAM, connect to 1.0V; V_{CCAUX} is FPGA auxiliary power supply pin, connect 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK14, BANK15~16, BANK34~35. On AC7050B FPGA core board, BANK34 and BANK35 need to be connected to DDR3, the voltage connection of BANK is 1.5V, and the voltage of other BANK is 3.3V. The VCCO of BANK15 and BANK16 is powered by the LDO, and can be changed by replacing the LDO chip.

Part 1.3: Active Differential Crystal

The AC7050B core board is equipped with a 50Mhz active differential crystal for the system's main clock of the FPGA. The crystal output is connected to the clock input pin of the FPGA (IO_L13P_T2_MRCC_14, Pin P15). This clock can be used to drive the user logic in the FPGA. Users can configure the FPGA's internal PLLs to achieve a higher clock.

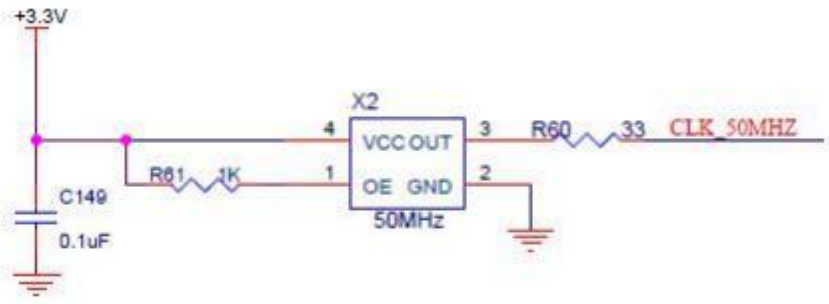

Figure 2-3-1: 50Mhz Active Crystal Oscillator

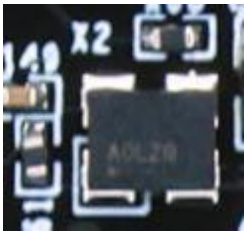

Figure 2-3-2: 50Mhz Active Crystal Oscillator on the Core Board

Clock Pin Assignment

Signal Name	FPGA PIN
CLK_50MHZ	P15

In addition, an active differential crystal is reserved on the AC7050B core board. The default is not installed. The differential crystal output is connected to the BANK34 global clock pin MRCC (AA6 and AB6) of the FPGA. Users can install their own clocks of different frequencies as needed.

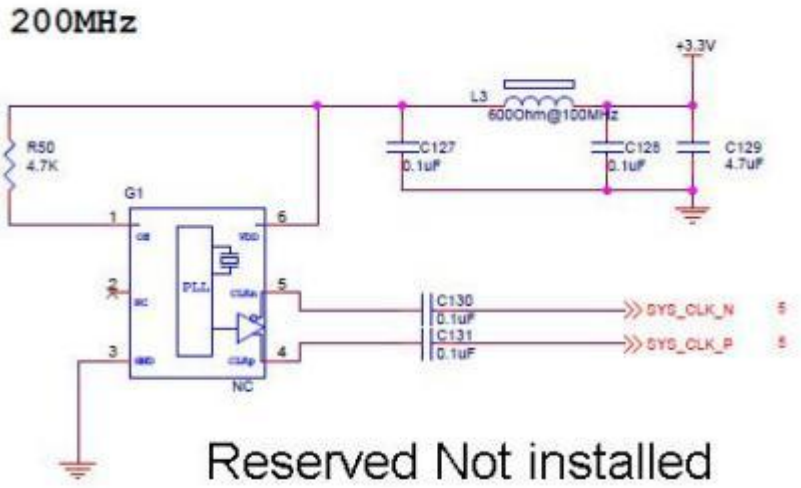

Figure 2-3-3: Reserved Active Differential Crystal

Reserved Differential Clock Pin Assignment

Signal Name	FPGA PIN
SYS_CLK_P	AA6
SYS_CLK_N	AB6

Part 1.4: DDR3 DRAM

The FPGA core board AC7050B is equipped with two Micron 4Gbit (512MB) DDR3 chips, model is MT41J256M16HA-125 (compatible with MT41K256M16HA-125). DDR bus width is a total of 32bit. The DDR3 SDRAM has a maximum operating speed of 333.3MHz (data rate 667Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 34 and BANK35 of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 2-4-1.

Bit Number	Chip Model	Capacity	Factory
U5,U6	MT41J256M16HA-125	256M x 16bit	Micron

Table 2-4-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

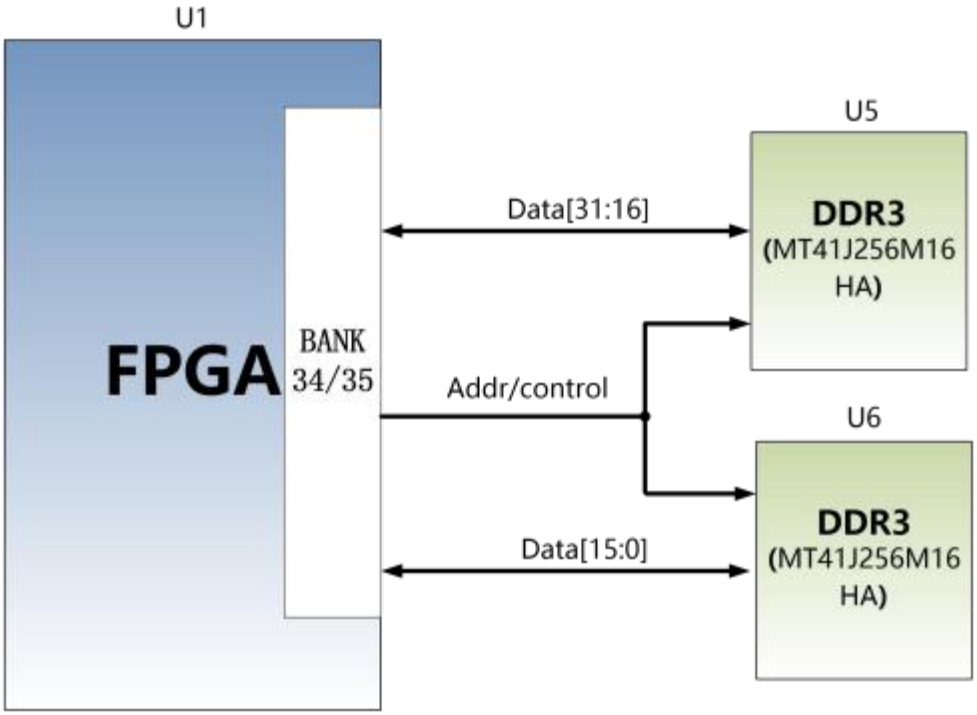

Figure 2-4-1: The DDR3 DRAM Schematic

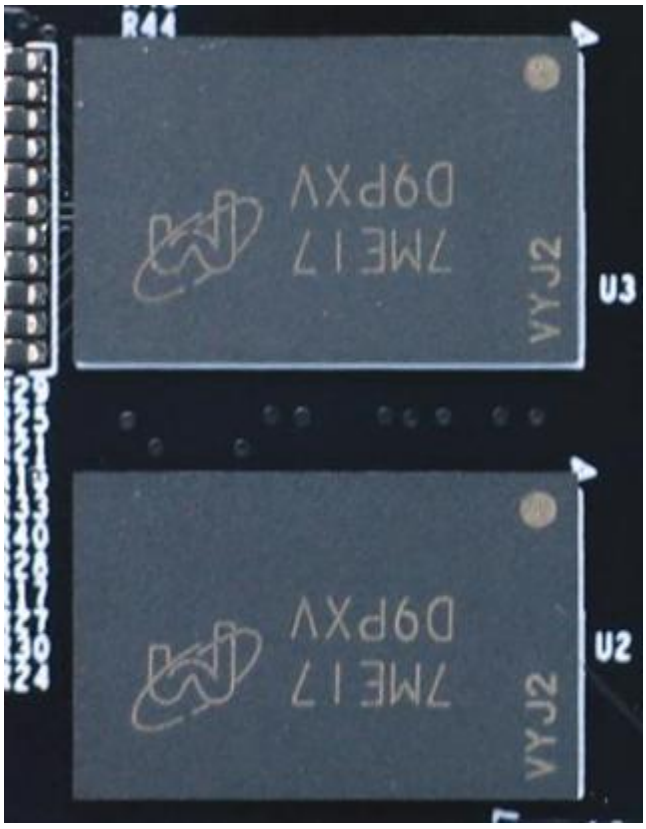

Figure 2-4-2: The DDR3 on the Core Board

DDR3 DRAM pin assignment:

Net Name	FPGA PIN Name	FPGA P/N
DDR3_DQS0_P	IO_L2N_T0_AD12N_35	J2
DDR3_DQS0_N	IO_L3P_T0_DQS_AD5P_35	J1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	L5
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	K5
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M2
DDR3_DQS2_N	IO_L15N_T2_DQS_35	M1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P6
DDR3_DQS3_N	IO_L21N_T3_DQS_35	N6
DDR3_DQ[0]	IO_L1N_T0_AD4N_35	H2
DDR3_DQ [1]	IO_L4N_T0_35	K2
DDR3_DQ [2]	IO_L2N_T0_AD12N_35	H3
DDR3_DQ [3]	IO_L5P_T0_AD13P_35	H6
DDR3_DQ [4]	IO_L5N_T0_AD13N_35	H5
DDR3_DQ [5]	IO_L6P_T0_35	K6
DDR3_DQ [6]	IO_L2P_T0_AD12P_35	H4
DDR3_DQ [7]	IO_L1P_T0_AD4P_35	J3
DDR3_DQ [8]	IO_L12P_T1_MRCC_35	M8
DDR3_DQ [9]	IO_L11P_T1_SRCC_35	L8
DDR3_DQ [10]	IO_L8N_T1_AD14N_35	L6
DDR3_DQ [11]	IO_L7P_T1_AD6P_35	J8
DDR3_DQ [12]	IO_L10N_T1_AD15N_35	K4
DDR3_DQ [13]	IO_L11N_T1_SRCC_35	K8
DDR3_DQ [14]	IO_L10P_T1_AD15P_35	L4
DDR3_DQ [15]	IO_L7N_T1_AD6N_35	J7
DDR3_DQ [16]	IO_L14P_T2_SRCC_35	L1
DDR3_DQ [17]	IO_L18P_T2_35	P3
DDR3_DQ [18]	IO_L14N_T2_SRCC_35	K1
DDR3_DQ [19]	IO_L16P_T2_35	N4
DDR3_DQ [20]	IO_L17N_T2_35	N1
DDR3_DQ [21]	IO_L17P_T2_35	P1
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	M3
DDR3_DQ [23]	IO_L16N_T2_35	N3
DDR3_DQ [24]	IO_L24N_T3_35	R4

DDR3_DQ [25]	IO_L23N_T3_35	R6
DDR3_DQ [26]	IO_L22P_T3_35	P7
DDR3_DQ [27]	IO_L20P_T3_35	N5
DDR3_DQ [28]	IO_L23P_T3_35	R7
DDR3_DQ [29]	IO_L22N_T3_35	N7
DDR3_DQ [30]	IO_L19P_T3_35	P8
DDR3_DQ [31]	IO_L24P_T3_35	R5
DDR3_DM0	IO_L4P_T0_35	K3
DDR3_DM1	IO_L8P_T1_AD14P_35	L7
DDR3_DM2	IO_L13P_T2_MRCC_35	M4
DDR3_DM3	IO_L20N_T3_35	M5
DDR3_A[0]	IO_L10N_T1_34	Y3
DDR3_A[1]	IO_L11N_T1_SRCC_34	U3
DDR3_A[2]	IO_L4P_T0_34	T5
DDR3_A[3]	IO_L2P_T0_34	T7
DDR3_A[4]	IO_L1P_T0_34	W5
DDR3_A[5]	IO_L2N_T0_34	T6
DDR3_A[6]	IO_L7N_T1_34	W1
DDR3_A[7]	IO_L4N_T0_34	U5
DDR3_A[8]	IO_L1N_T0_34	W4
DDR3_A[9]	IO_L14P_T2_SRCC_34	Y6
DDR3_A[10]	IO_L14N_T2_SRCC_34	Y5
DDR3_A[11]	IO_L8P_T1_34	W2
DDR3_A[12]	I O_L9N_T1_DQS_34	U1
DDR3_A[13]	IO_L11P_T1_SRCC_34	U4
DDR3_A[14]	IO_L15P_T2_DQS_34	Y4
DDR3_BA[0]	IO_L8N_T1_34	Y1
DDR3_BA[1]	IO_L9P_T1_DQS_34	U2
DDR3_BA[2]	IO_L10P_T1_34	W3
DDR3_S0	IO_L7P_T1_34	V1
DDR3_RAS	IO_L5P_T0_34	V7
DDR3_CAS	IO_L6P_T0_34	T8
DDR3_WE	IO_L6N_T0_VREF_34	U8
DDR3_ODT	IO_L5N_T0_34	V6
DDR3_RESET	IO_L17N_T2_34	AA1
DDR3_CLK_P	IO_L12P_T1_MRCC_34	T3

DDR3_CLK_N	IO_L12N_T1_MRCC_34	T2
DDR3_CKE	IO_L3N_T0_DQS_34	V4

Part 1.5: QSPI Flash

The FPGA core board AC7050B is equipped with one 128MBit QSPI FLASH, and the model is N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, core application code and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-5-1.

Position	Model	Capacity	Factory
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1: QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip select signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 2-5-1 shows the hardware connection of QSPI Flash.

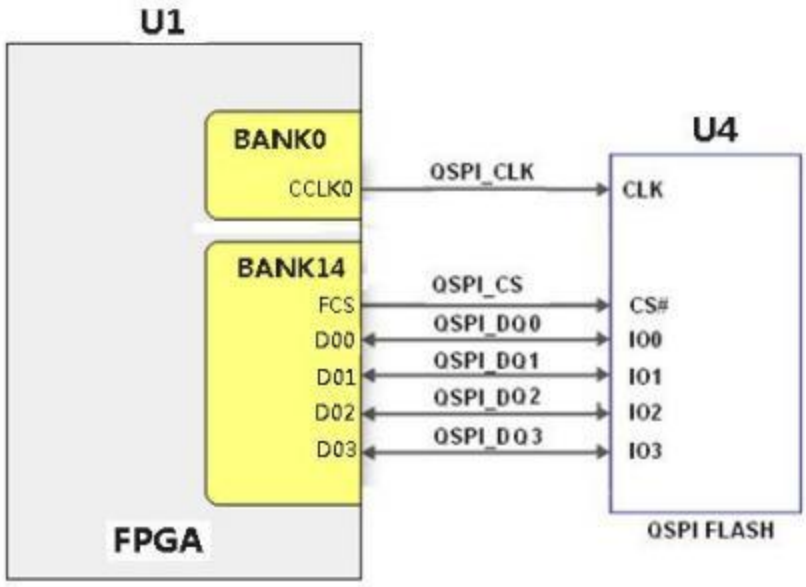

Figure 2-5-1: QSPI Flash Schematic

QSPI Flash pin assignments:

Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	D9
QSPI_CS	IO_L6P_T0_FCS_B_14	N17
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	M21
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	M22
QSPI_DQ2	IO_L2P_T0_D02_14	N21
QSPI_DQ3	IO_L2N_T0_D03_14	N22

Figure 2-5-1: QSPI on the Core Board

Part 1.6: LED Light on Core Board

There are 3 red LED lights on the AC7050B FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. The user LED light is connected to the IO of the BANK16, the user can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED is off. When the connection IO voltage is low, the user LED will be lit. The schematic diagram of the LED light hardware connection is shown in Figure 2-6-1:

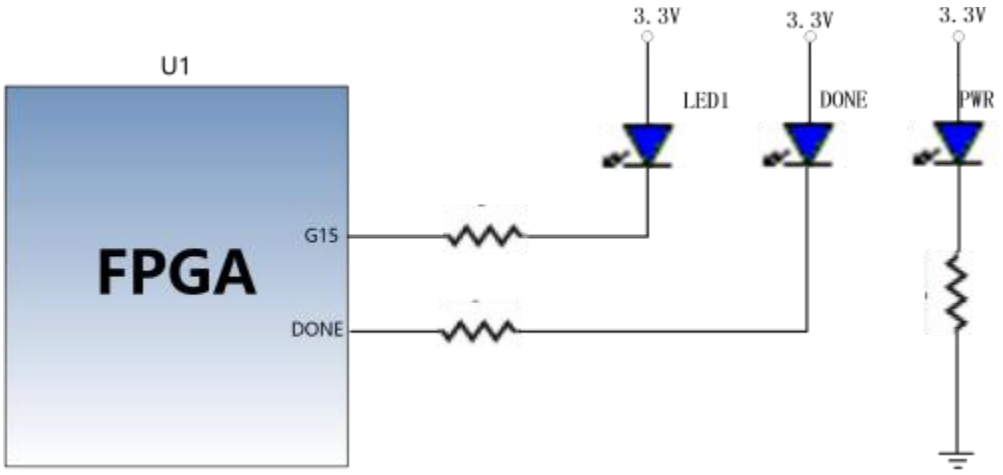

Figure 2-6-1: LED lights on core board Schematic

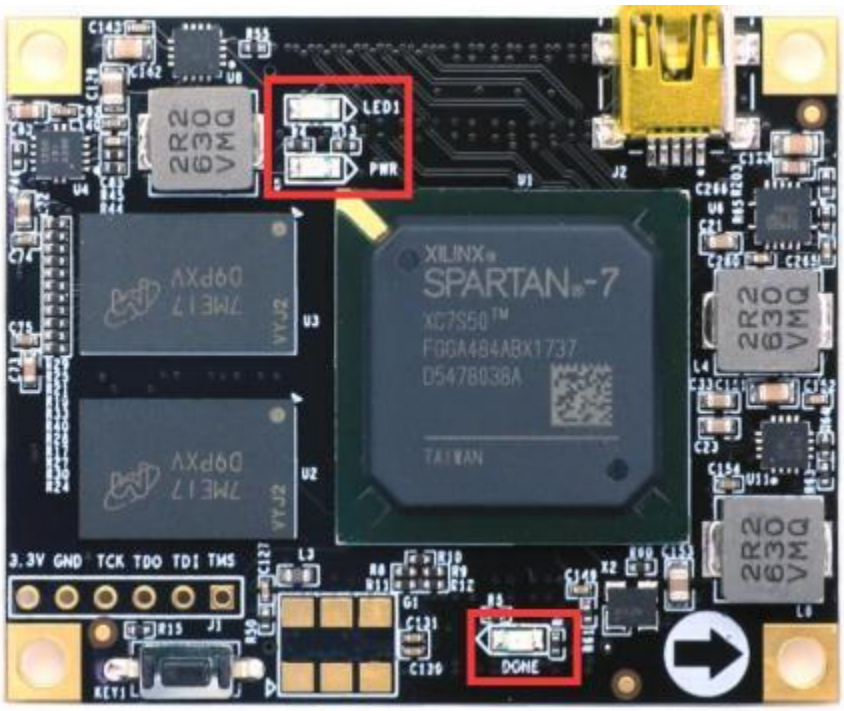

Figure 2-6-2: LED lights on the Core Board

User LEDs Pin Assignment

Signal Name	FPGA Pin Number	Description
LED1	G15	User LED

Part 1.7: JTAG Interface

The JTAG test socket J1 is reserved on the AC7050B core board for JTAG download and debugging when the core board is used alone. Figure 2

-7-1 is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK, GND, +3.3V these six signals.

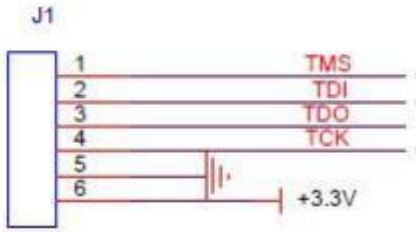

Figure 2-7-1: JTAG Interface Schematic

The JTAG interface J1 on AC7050B FPGA core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connection to debug on the core board, you need to solder a 6-pin single-row pin header. Figure 2-8-2 shows the JTAG interface J1 on the AC7100 FPGA core board.

Figure 2-6-2 JTAG Interface on Core Board

Part 1.8: Power Interface on the Core Board

In order to make the AC7050B FPGA core board work alone, the core board is reserved with a Mini USB interface, and the USB port is connected to the USB port of the computer to supply +5V power to the core board. This allows the user to debug the functionality of the AC7050B FPGA core board without the need for Carrier Board. The interface of the Mini USB port on the core board is J2. When the user supplies power to the core board through the Mini USB port (J2), it cannot be powered through the Carrier Board. Otherwise, current conflict may occur and the USB interface of the computer may be burned out.

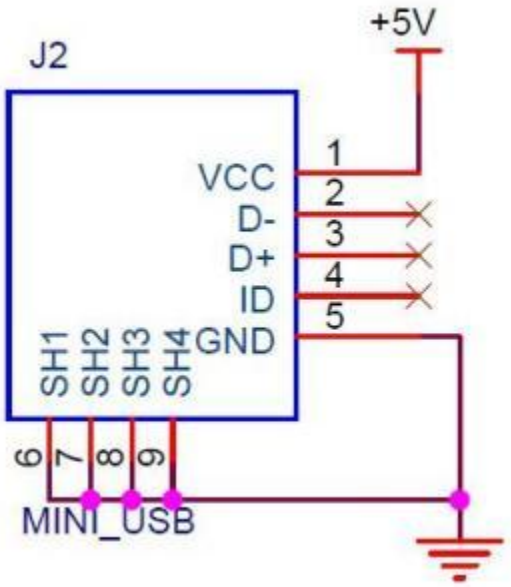

Figure 2-8-1：MINI USB interface schematic

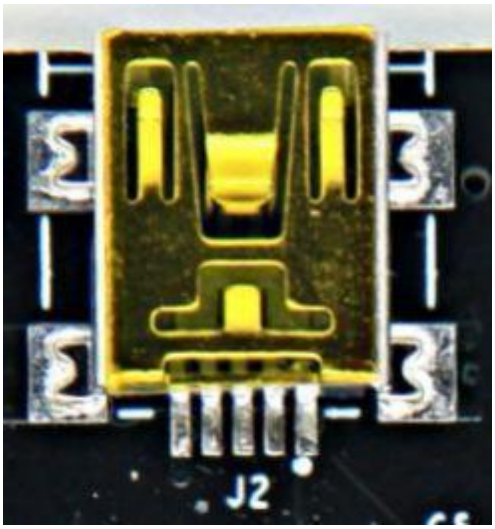

Figure 2-8-2：MINI USB interface on the Core Board

Part 1.9: Board to Board Connectors pin assignment

The core board has a total of two high-speed board to board connectors. The core board uses two 80-pin inter-board connecters to connect to the Carrier Board. The IO port of the FPGA is connected to the two connecters by differential routing. The pin spacing of the connectors is 0.5mm, insert to the board to board connectors on the Carrier Board for high-speed data communication.

Board to Board Connectors CON1

The 80-pin board to board connectors CON1, which is used to connect the normal IO of FPGA (which contains 6 pairs of differential interface IO, can be used as LVDS data communication), the default IO level is 3.3V. The pin assignment of the CON1 expansion port is shown in Table 2-9-1.

Pin Assignment of Board to Board Connectors CON1

CON1 PIN	Net Name	FPGA PIN	Input/ Output	CON1 PIN	Net Name	FPGA PIN	Input/ Output
PIN1	B15_L10_P	E22	I/O	PIN2	B15_L11_P	F21	I/O
PIN3	B15_L10_N	D22	I/O	PIN4	B15_L11_N	F22	I/O
PIN5	B15_L7_P	B21	I/O	PIN6	B15_L20_P	G21	I/O
PIN7	B15_L7_N	B22	I/O	PIN8	B15_L20_N	G22	I/O
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B15_L9_P	D21	I/O	PIN12	B15_L12_P	F19	I/O
PIN13	B15_L9_N	C22	I/O	PIN14	B15_L12_N	F20	I/O
PIN15	B15_L8_P	D20	I/O	PIN16	B16_L24_P	E19	I/O
PIN17	B15_L8_N	C20	I/O	PIN18	B16_L24_N	D19	I/O
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B16_L20_P	C19	I/O	PIN22	B16_L22_P	E17	I/O
PIN23	B16_L20_N	B19	I/O	PIN24	B16_L22_N	E18	I/O
PIN25	B16_L19_P	D18	I/O	PIN26	B16_L16_P	E15	I/O
PIN27	B16_L19_N	C18	I/O	PIN28	B16_L16_N	E16	I/O
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B16_L15_P	D16	I/O	PIN32	B16_L6_P	G14	I/O
PIN33	B16_L15_N	C17	I/O	PIN34	B16_L6_N	F15	I/O
PIN35	B16_L13_P	C15	I/O	PIN36	B16_L4_P	F13	I/O
PIN37	B16_L13_N	C16	I/O	PIN38	B16_L4_N	F14	I/O
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B16_L23_N	A20	I/O	PIN42	B16_IO0	G13	I/O
PIN43	B16_L23_P	B20	I/O	PIN44	B16_L17_N	A14	I/O
PIN45	GND	-	Ground	PIN46	B16_L17_P	B14	I/O
PIN47	B16_L21_N	A19	I/O	PIN48	B16_L7_N	C13	I/O
PIN49	B16_L21_P	A18	I/O	PIN50	B16_L7_P	D13	I/O
PIN51	GND	-	Ground	PIN52	GND	-	Ground

PIN53	B16_L18_N	A17	I/O	PIN54	B16_L11_P	D14	I/O
PIN55	B16_L18_P	A16	I/O	PIN56	B16_L11_N	D15	I/O
PIN57	GND	-	Ground	PIN58	B16_L12_P	D12	I/O
PIN59	B16_L14_N	B16	I/O	PIN60	B16_L12_N	C12	I/O
PIN61	B16_L14_P	B15	I/O	PIN62	B16_L5_N	E12	I/O
PIN63	GND	-	Ground	PIN64	GND	-	Ground
PIN65	B16_L9_N	A13	I/O	PIN66	B16_L5_P	F12	I/O
PIN67	B16_L9_P	B13	I/O	PIN68	B16_L3_N	D11	I/O
PIN69	GND	-	Ground	PIN70	B16_L3_P	E11	I/O
PIN71	B16_L8_N	A12	I/O	PIN72	B16_L1_N	F11	I/O
PIN73	B16_L8_P	A11	I/O	PIN74	B16_L1_P	G11	I/O
PIN75	GND	-	Ground	PIN76	GND	-	Ground
PIN77	B16_L10_N	C11	I/O	PIN78	B16_L2_N	F10	I/O
PIN79	B16_L10_P	C10	I/O	PIN80	B16_L2_P	G10	I/O

The pins of B16_L23_P/N, B16_L21_P/N, B16_L18_P/N, B16_L14_P/N, B16_L9_P/N and B16_L8_P/N are differentially derived on the PCB and can be used as high-speed LVDS data communication.

Figure 2-9-1: Board to Board Connectors CON1 on the Core Board

Board to Board Connectors CON2

The 80-pin board to board connectors CON1, which is used to connect to +5V power supply, JTAG interface signal and the normal IO of FPGA (which contains 6 pairs of differential interface IO, can be used as LVDS data communication), the default IO level is 3.3V. The pin assignment of the CON2 expansion port is shown in Table 2-9-2

Pin Assignment of Board to Board Connectors CON2

CON2 PIN	Net Name	FPGA PIN	Input/ Output	CON2 PIN	Net Name	FPGA PIN	Input/ Output
PIN1	+5V	-	Power	PIN2	+5V	-	Power
PIN3	+5V	-	Power	PIN4	+5V	-	Power
PIN5	+5V	-	Power	PIN6	+5V	-	Power
PIN7	+5V	-	Power	PIN8	+5V	-	Power
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B14_L4_N	P22	I/O	PIN12	B14_L5_P	N20	I/O
PIN13	B14_L4_P	P21	I/O	PIN14	B14_L5_N	P20	I/O
PIN15	B14_L7_N	T22	I/O	PIN16	B14_L20_N	AA22	I/O
PIN17	B14_L7_P	T21	I/O	PIN18	B14_L20_P	Y22	I/O
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B14_L9_P	U22	I/O	PIN22	B14_L22_N	AB21	I/O
PIN23	B14_L9_N	V22	I/O	PIN24	B14_L22_P	AA21	I/O
PIN25	B14_L8_N	W22	I/O	PIN26	B14_L23_P	AB19	I/O
PIN27	B14_L8_P	V21	I/O	PIN28	B14_L23_N	AB20	I/O
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B14_L24_N	V19	I/O	PIN32	B14_L19_P	Y20	I/O
PIN33	B14_L24_P	V18	I/O	PIN34	B14_L19_N	AA20	I/O
PIN35	B14_L12_N	U19	I/O	PIN36	B14_L21_P	W18	I/O
PIN37	B14_L12_P	U18	I/O	PIN38	B14_L21_N	Y19	I/O
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B14_L15_N	U17	I/O	PIN42	B15_L14_N	M18	I/O
PIN43	B14_L15_P	T17	I/O	PIN44	B15_L14_P	M17	I/O
PIN45	B14_L16_N	R17	I/O	PIN46	GND	-	Ground
PIN47	B14_L16_P	R16	I/O	PIN48	B15_L16_N	K19	I/O
PIN49	B14_IO0	N15	I/O	PIN50	B15_L16_P	K18	I/O
PIN51	GND	-	Ground	PIN52	GND	-	Ground
PIN53	B14_L14_N	R18	I/O	PIN54	B15_L5_N	J16	I/O
PIN55	B14_L14_P	P17	I/O	PIN56	B15_L5_P	K16	I/O
PIN57	B14_L10_N	Y21	I/O	PIN58	GND	-	Ground
PIN59	B14_L10_P	W21	I/O	PIN60	B15_L13_N	L15	I/O
PIN61	B14_L11_N	V20	I/O	PIN62	B15_L13_P	M15	I/O
PIN63	GND	-	Ground	PIN64	GND	-	Ground
PIN65	B14_L11_P	U20	I/O	PIN66	B15_L6_N	J15	I/O

PIN67	B14_L18_N	T20	I/O	PIN68	B15_L6_P	K15	I/O
PIN69	B14_L18_P	T19	I/O	PIN70	GND	-	Ground
PIN71	B14_L17_N	R20	N.C.	PIN72	B15_L4_N	G16	I/O
PIN73	B14_L17_P	R19	N.C.	PIN74	B15_L4_P	H16	I/O
PIN75	GND	-	Ground	PIN76	GND	-	Ground
PIN77	TDI	W9	O	PIN78	TCK	G9	O
PIN79	TMS	Y10	O	PIN80	TDO	W10	I

The pins of B15_L14_P/N, B15_L16_P/N, B15_L5_P/N, B15_L13_P/N, B15_L6_P/N and B15_L4_P/N are differentially derived on the PCB and can be used as high-speed LVDS data communication.

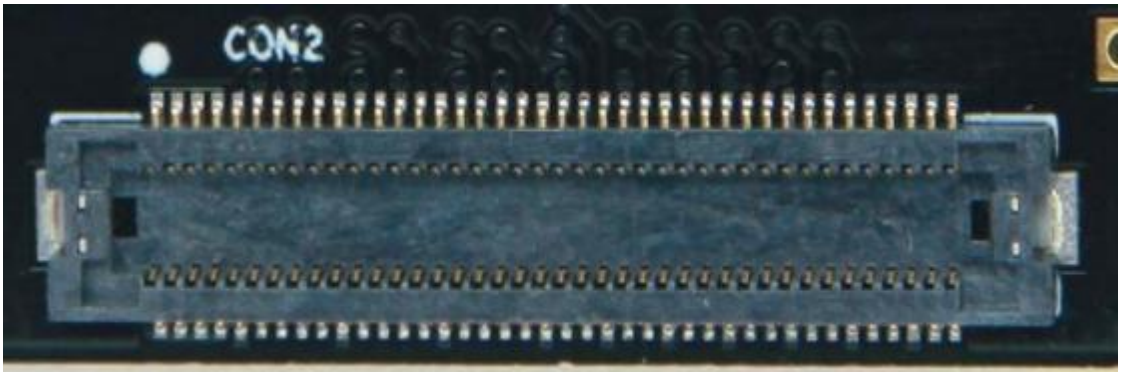

Figure 2-9-2: Board to Board Connectors CON1 on the Core Board

Part 1.10: Power Supply

The AC7050B FPGA core board is powered by DC5V via Carrier Board, and it is powered by the Mini USB interface when it is used alone. Please be careful not to supply power to the Mini USB and the Carrier Board at the same time to avoid damage. The power supply design diagram on the board is shown in Figure 2-10-1.

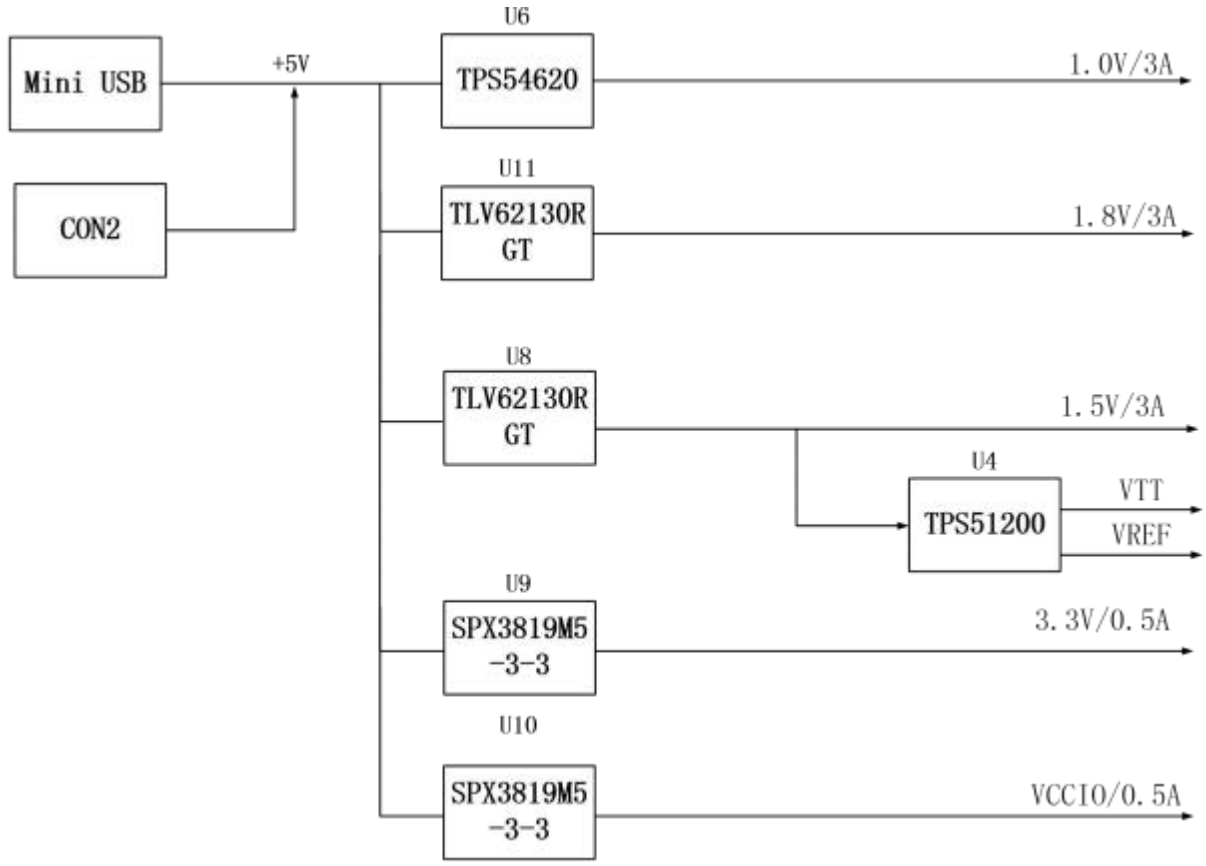

Figure 2-10-1：Power Supply on core board schematic

The core board is powered by +5V, converted to +1.0V by a 1 channel DC/DC power chip TPS54620, and the output current can be as high as 6A. It is converted into +1.8V and +1.5V power supply through 2 DC/DC power chip TLV62130RGT, and the output current can be up to 3A per channel. In addition, VCCIO power supply and +3.3V power supply are generated by 2-way LDO SPX3819M5-3-3. VCCIO mainly supplies power to BANK15 and BANK16 of FPGA. Users can adapt other voltages of BANK15,16 to different voltages by replacing other LDO chips. The standard allows differential signals connected to BANK15 and BANK16 to implement LVDS data communication at different level standards. The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	FPGA Core Voltage

+1.8V	FPGA auxiliary voltage
+3.3V	VCCIO of Bank0 and Bank14 of FPGA,QSIP FLASH, Clock Crystal
+1.5V	DDR3, Bank34 and Bank35 of FPGA
VREF,VTT(+0.75V)	DDR3
VCCIO(+3.3V)	FPGA Bank15, Bank16

The power circuit on the AC7050B FPGA core board is shown in Figure 2-11-2 and Figure 2-11-3

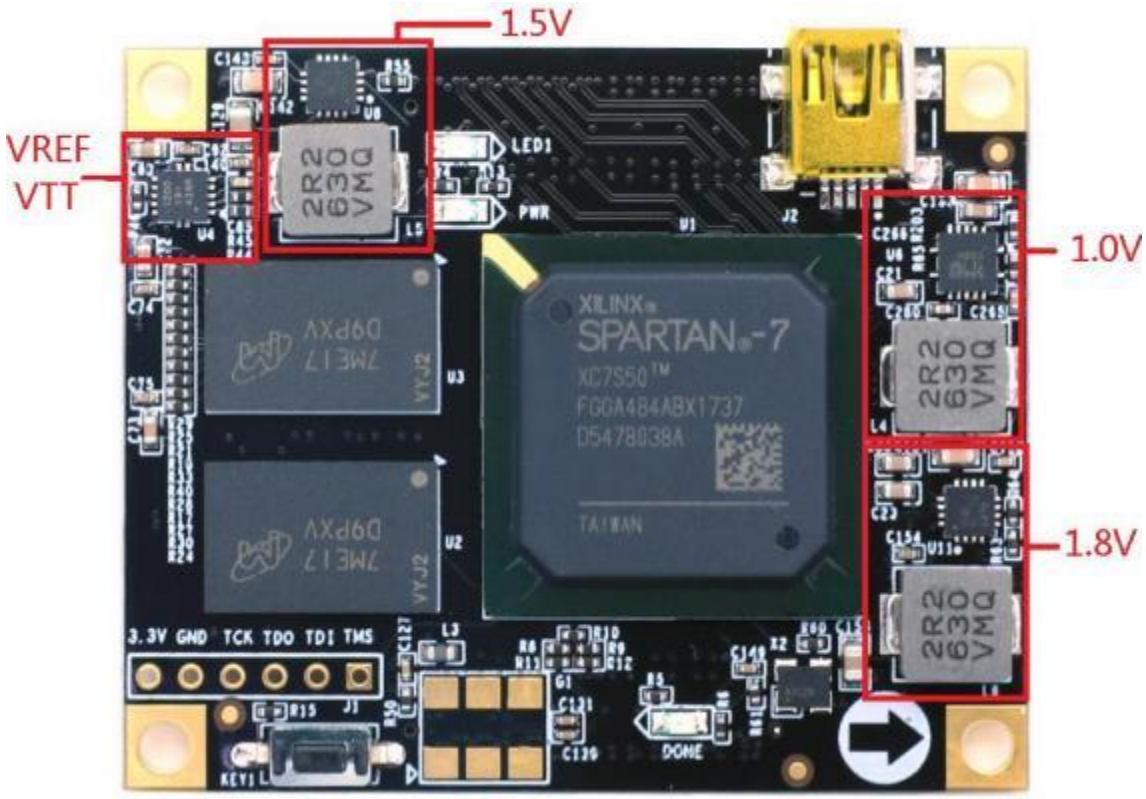

Figure 2-11-2: Power Supply on the AC7050B FPGA Core Board (Top View)

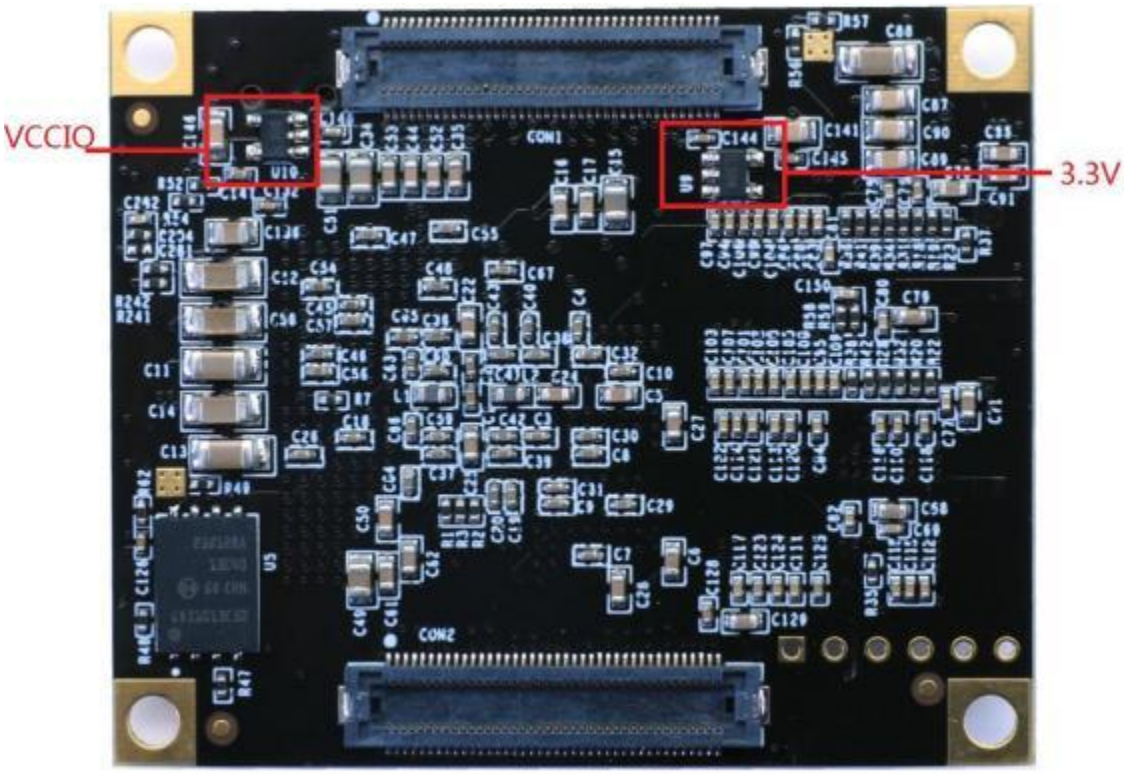

Figure 2-11-3: Power Supply on the AC7050B FPGA Core Board (Bottom View)

Part 1.12: Structure Diagram

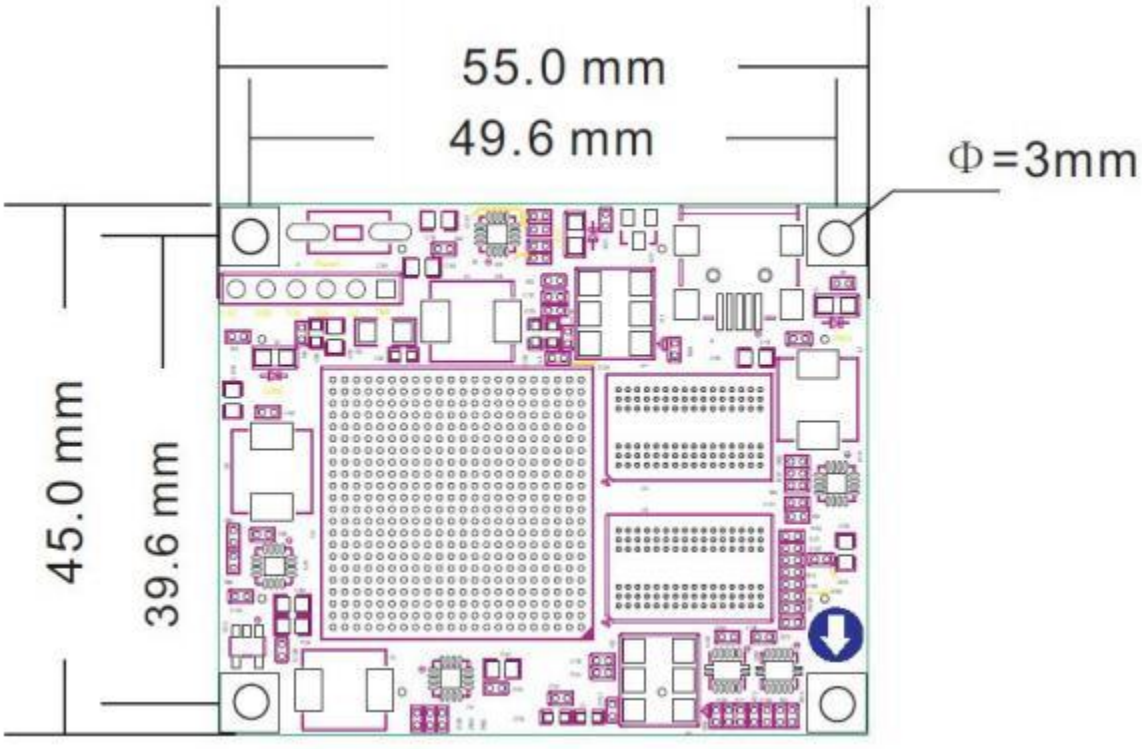

Figure 2-12-1: AC7050B FPGA Core board (Top view)

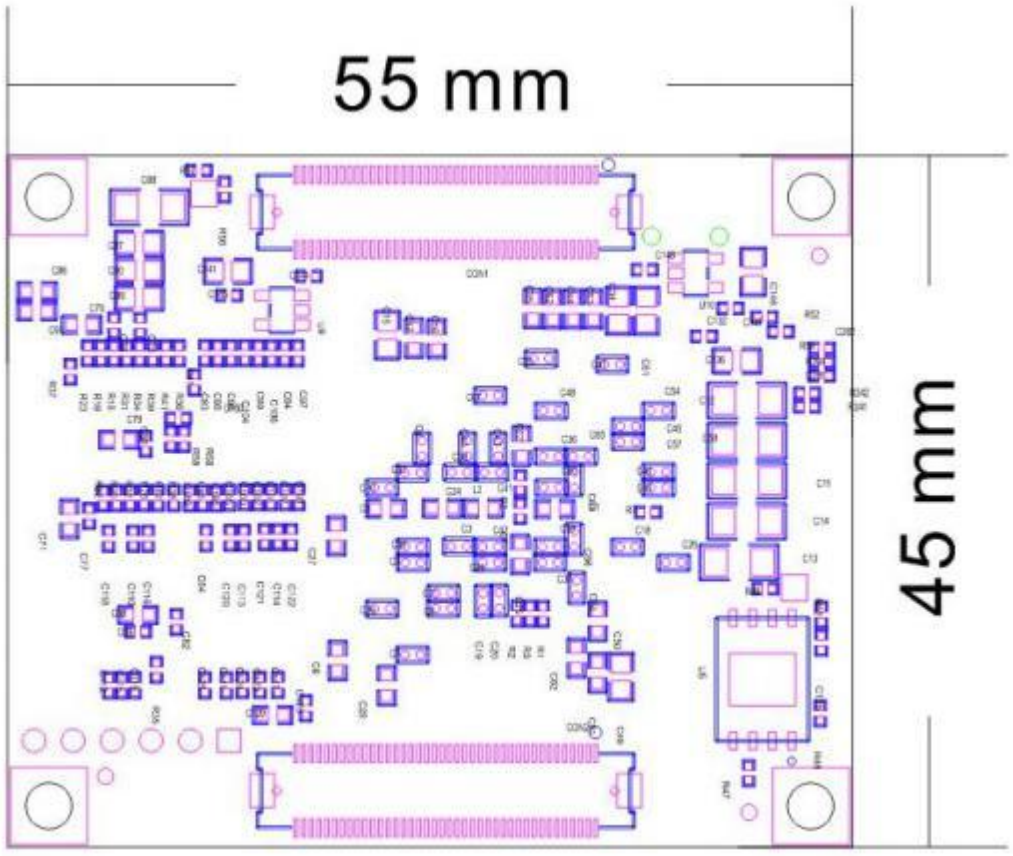

Figure 2-12-2: AC7050B FPGA Core board (Bottom view)